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Art Unit: 2614
Tuesday, March 30, 2004

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From: Pamela Reynolds
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Pamela.Reynolds@uspto.gov

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SEARCH REQUEST FORM

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Requester's Full Name: Brian P. Yenke Examiner # : 77730 Date: 29 March 2004
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Title of Invention: High Speed Video Frame Buffer

Inventors (please provide full names): Robert J. Proebsting

Earliest Priority Filing Date: 09 Aug 96

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

- (Sense Amplifiers) near AND (shared or used) near (Adjacent Arrays or adjoining Arrays)
- (integrate or include or combine) near (memory AND controller) near (IC or chip or circuit)
- (store or place) near (row or line) near (non-adjoining or non-adjacent) near (Arrays)

1:00

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L1: Entry 4 of 15 File: TDBD Jul 1, 1992

TDB-ACC-NO: NN9207383

DISCLOSURE TITLE: Video Frame Buffer with Increased Performance Capability.

Page mode
screen row
memory row

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, July 1992, US

VOLUME NUMBER: 35
ISSUE NUMBER: 2
PAGE NUMBER: 383 - 388

PUBLICATION-DATE: July 1, 1992 (19920701)

CROSS REFERENCE: 0018-8689-35-2-383

DISCLOSURE TEXT:

- The memory organization of the frame buffer is the limiting factor to the update performance of frame buffered raster scan displays. The memory organization determines how many and which pixels can be accessed in a single memory cycle, and hence limits the number of pixels that can be updated in parallel by the update hardware. High performance displays frequently allow parallel update to the frame buffer, effectively resulting in a lower memory cycle time per pixel. - The parallel update required is clearly dependent upon the size and shape of the objects being drawn into the frame buffer as well as the memory available and the memory technology. There are several frame buffer organizations that allow the parallel access of several pixels if they are in a horizontal line or if they are in an arbitrary square. - The implementation of memory organizations determines the cost and complexity of frame buffered systems and their associated update hardware. The memory organizations and their implementations hence become critical in determining the cost and functionality of frame buffered displays. Because of the nature of memory chips, the complexity of the frame buffer organization is uniquely determined by the number of memory chips and the number of unique signal wires connected to them. These wires are the address wires (usually multiplexed into Row Address and Column Address signals), data wires, and the control signals (Row Address Strobes, Column Address Strobes, and the Write Enables). - A frame buffer organization which allows the access of 16 arbitrarily aligned horizontal pixels is described in (1). This is achieved by using 16 memory chips (64 Kilobits each) to realize a 1K by 1K frame buffer. The ability to access an arbitrarily aligned word is achieved by strobing different column addresses to different chips depending upon the left boundary of the desired word. The implementation uses one address bus, but 16 column address strobe wires. The first address is driven and the appropriate chips strobed, followed by the second address and the strobe of the rest of the chips. This implementation requires a longer memory cycle but only 8 address signals. - To optimize the access for different operations, the access to an 8 by 8 array of pixels that could be arbitrarily aligned was implemented in (2). The 8 by 8 display had eight sets of address buses (8 wires each) which could deliver different addresses to different columns of the 8 by 8 array of memory chips. The memory organization used provided different row addresses by using the same address wires and providing different column strobes, and provided different column addresses by driving different addresses on different columns. - Another complication is a number of data signals. In the 8 by 8 display example, an 8-bit-per-pixel frame buffer would drive 512 bits of data. Obviously, such number of bits can be processed only by an array of processors, or require additional multiplexers, which shrink down the number of bits read from the frame buffer to the size of data bus. In case of medium-cost or low-cost displays such number of I/O and address lines is too large to be accepted by 16/32 bit general processors or even specialized display controllers. - This article describes a frame buffer, which has a

reduced number of I/O and address lines, but still allows full all-point addressability, while allowing simultaneous access of up to five pixels for increased drawing speed. In a vertical or diagonal direction, up to four pixels can be accessed simultaneously. - This description is going to assume a frame buffer with an 1280 by 1024 resolution with eight bits per pixels. The design parameters can be extended to frame buffers with different resolutions and different number of bits per pixel. - In a video display adapter where cost and size are critical, it is important to use a memory technology that requires the fewest integrated circuits to obtain the required memory. This required the new 256Kx4 video memory chips. Using the 256Kx4 memories prevented adapting a scheme such as that described in been3|. This frame buffer can be built using 10 memory chips, each having a capacity of 256K by 4 bits. - The memory organization referred to in this article is shown in Fig. 1. - Each pair of memory modules share the same control and address lines, with the exception of two address lines as described later. The data from each pair is accessed as eight bits. The five pairs are referred to as Module A through Module E. The serial output of the memory is sent to a video digital-to-analog converter and displayed on the screen. - Each location in the five pair of memory modules corresponds to a pixel location on the 1280 x 1024 display screen. Horizontal vectors can be written five pixels at a time because each horizontally adjacent pixel is contained in a separate module. The data lines are brought into each memory module pair separately from the others. In this particular configuration there are forty separate data lines. Write enable lines are also wired separate to the five memory module pairs. The screen is divided up into 512 sections or pages with each page having a row address as shown in Fig. 2. - Each of these pages is full screen wide by 2 pixels high. One significant feature of a page is that multiple memory accesses within a page can be done at a faster rate. Each memory access requires a row address and a column address. If the row address does not change from one memory access to another, a memory cycle called a page mode cycle can be done in less time. The configuration described here permits most horizontal lines or vectors to be written in page mode. - The column addresses for the video memory changes for each five pixels in the horizontal direction within the page as shown in Fig. 3. Each box in the figure represents a screen area of one pixel in height by five pixels in length. - A unique feature of the memory organization covered in this article is the pixel interleaving within the memory. Within the screen rows, the memory module that contains a particular pixel is interleaved on a modulo 5 basis from row to row. This is shown in Fig. 4. - The interleaving facilitates fast vector writes in vertical as well as horizontal directions. As previously explained the horizontal writing speed is improved because any group of five pixels on a horizontal line are contained in five separate memory modules. In the vertical direction, note that the pixels are also contained in separate modules. In order to maximize the vertical drawing rate, and minimize the amount of address lines going into the frame buffer, two address lines are individually controlled while seven other lines are wired in common to all the memory modules. The two address lines that are separately controlled are the least significant, (MA0) and the most significant (MA8). Careful study of Figs. 2 and 3 will reveal that a row address to the memory is actually two screen rows. Within a memory row any two vertically adjacent pixels have column addresses that differ in the most significant address only. For example, a pixel in column memory row 3 has a pixel with column memory row 259 directly above. Since each screen row also has the interleaving factor, the two pixels can be addressed simultaneously. Furthermore, any two memory rows starting on an even address differ in only the least significant address bit, allowing writes to four vertically adjacent pixels in one memory cycle. A similar analysis can be made for diagonal vectors which essentially consist of a combination of horizontally and vertically adjacent pixels. - Described is a memory organization designed for use in low-cost high-performance video adapters. The unique features incorporated in the organization are applicable to other video frame buffers. - This memory organization allows the control of writing individual pixels in this array by controlling the write enable pins to each memory chip directly. - The data wires in this memory organization are separated such that up to five horizontal pixels can be read or written in one memory cycle. This leads to faster vector write times to the screen. - The data wires and address wires in this memory organization are separated such that up to four vertical pixels can be read or written in one memory cycle. This leads to faster vector write times to the screen. - In addition to the above mentioned technique for rapidly accessing successive pixels, the memory organization also allows for access of horizontally adjacent pixels in page mode. Page mode can be used if these successive pixels have the same memory row address. In this configuration, all pixels in any screen row have the same memory row address. - Other configurations are possible by separating more address lines, which would allow simultaneous access of more than four pixels vertically. The above concepts are also applicable to

organizations with other than the most and least significant address lines wired separately to each memory module pair. - The feature of interleaving pixels vertically allows simultaneous access of up to four pixels in a vertical direction. This concept is also applicable to interleaving factors other than two as described. - The above concepts are also applicable to other organizations with a different size (e.g,. 2048 by 1280, etc.). This could result in being able to access more than five pixels simultaneously. - References (1) U.S. Patent 4,435,792. (2) R. F. Sproull, I. E. Sutherland, A. Thompson, S. Gupta and C. Minter, "The 8 by 8 Display," ACM Trans. Graphics 2, 1, 32-56 (January 1983). (3) U.S. Patent 4,903,217.

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File 344:Chinese Patents Abs Aug 1985-2004/Mar
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DIALOG(R)File 350:Derwent WPIX

012288224
WPI Acc No: 1999-094330/199908
XRPX Acc No: N99-068596
High speed video frame **buffer - has memory circuit having array remaining opening when address is selected until different row in same array or adjacent array is selected**
Patent Assignee: TOWNSEND & TOWNSEND & CREW LLP (TOWN-N)
Inventor: **PROEBSTING R J**
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 340225	A	19980911	TW 97111246	A	19970806	199908	B
KR 98018536	A	19980605	KR 9737997	A	19970808	199923	
US 6026044	A	20000215	US 9623955	A	19960809	200016	
			US 97884845	A	19970630		
US 6031783	A	20000229	US 9623955	A	19960809	200018	
			US 97884845	A	19970630		
			US 98179260	A	19981026		

Priority Applications (No Type Date): US 9623955 P 19960809; US 97884845 A 19970630; US 98179260 A 19981026
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 340225	A		6	G11C-008/02	
KR 98018536	A			G06F-003/14	
US 6026044	A			G11C-008/00	Provisional application US 9623955
US 6031783	A			G11C-007/00	Provisional application US 9623955
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High speed video frame **buffer...**
Inventor: **PROEBSTING R J**
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1 **A 16K × 1 bit dynamic RAM**
Schroeder, P.; Proebsting, R.;
Solid-State Circuits Conference. Digest of Technical Papers. 1977 IEEE International ,Volume: XX , Feb 1977
Pages:12 - 13

[Abstract] [PDF Full-Text (496KB)] **IEEE CNF**

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2 **A TTL compatible 4096-bit N-channel RAM**
Proebsting, R.; Green, R.;
Solid-State Circuits Conference. Digest of Technical Papers. 1973 IEEE International ,Volume: XVI , Feb 1973
Pages:28 - 29

[Abstract] [PDF Full-Text (336KB)] **IEEE CNF**

SESSION I: MOS MEMORIES

Chairman: *William Lattin*
Intel Corp.
Santa Clara, CA

WAM 1.1: A 16K x 1 Bit Dynamic RAM

Paul R. Schroeder and Robert J. Proebsting
Mostek Corp.
Carrollton, TX

A 16K x 1 BIT dynamic RAM capable of 150-ns access time has been developed using a two-level N-channel polysilicon gate process and a single transistor cell. Utilizing the standard 16-pin package configuration, seven address bits are multiplexed. All clocks and other inputs are TTL compatible. Maximum user flexibility has been provided by incorporating ±10% supplies, a nonlatched tri-state data output controlled by $\overline{\text{CAS}}$, a wide multiplex timing window, page mode capability, and $\overline{\text{RAS}}$-only refresh.

A block diagram of the circuit is shown in Figure 1 and a photograph of a fabricated device appears in Figure 2. The chip is organized internally as a single 128 x 128 balanced array with both column decoders and sense amplifiers located in a row through the center of the array. To maintain a balanced configuration, each column decode circuit is divided into two parts with one half on either side of the sense amplifiers. These column decoders provide 1 of 64 selection. The final 1 of 128 column decoding is accomplished by selection of one of two pairs of data, $\overline{\text{data}}$ buses which also run through the center, and which are used for I/O coupling to the selected digit circuits. Since access is provided to both the true and complement sense lines associated with each amplifier, no digit pullup transistors are required. This permits completely dynamic flipflop type detectors to be used, resulting in very low power consumption.

The basic digit circuit – Figure 3 – consists of sense amplifier, memory cells, reference cell, and input-output coupling. Each sense amplifier is shared by 128 cells, 64 on each side (plus reference cell). Dimensions of the double-poly cell[1,2] are approximately 14.5 μm x 30 μm. Cell and digit line capacitances are estimated to be 0.04 pF and 0.8 pF, respectively.

A single set of seven address buffers is used for both row and column addresses in a multiplexed mode. A set of switches connects the address and address complement lines running through the row decoder to corresponding lines in the column decoders. During row address decoding time, these switches are left in the open circuit condition so that signals generated by the input buffers are coupled onto the row decode address lines only. Once row decoding is completed, row select information is trapped dynamically in the row decoder circuits, the address input buffers are reset, and the switches are closed in preparation for receiving column address information. At column address time the address lines, going now to both row and column decode circuits, are activated with column address signals. Column decoding takes place in the usual fashion. The row decoders, however, are effectively disabled at this time so that the previously completed row selection is undisturbed. A schematic of the row decoder circuit is shown in Figure 4.

This decoder architecture is a logical modification of earlier work implemented in a 4K RAM where both the input buffers and decoders are multiplexed. The higher density memory array used in the present 16K design, however, makes the use of a single multiplexed decoder for both row and column selection impractical.

To provide wide operating margins and noise immunity desired by users, a special input stage was designed to detect the TTL input levels. A circuit schematic of this stage is shown in Figure 5. Differential detection with a 1.5-V reference level is employed to maximize noise margin and avoid dependence on device threshold and other process parameters.

In the Figure 5 circuit, a positive common mode voltage boost is capacitively coupled to the gates of transistors T3 and T4 to assure that at least one of these is turned on at latch time, even though both the input and reference voltages may be less than the device threshold voltage. The addition of T1 and C1 in the V_{IN} path helps to increase the amount of negative undershoot on V_{IN} which can be tolerated between the time TA goes low and the time latching takes place. This is necessary to avoid a long row address hold time which would otherwise be required.

Key device characteristics are summarized in Figure 6.

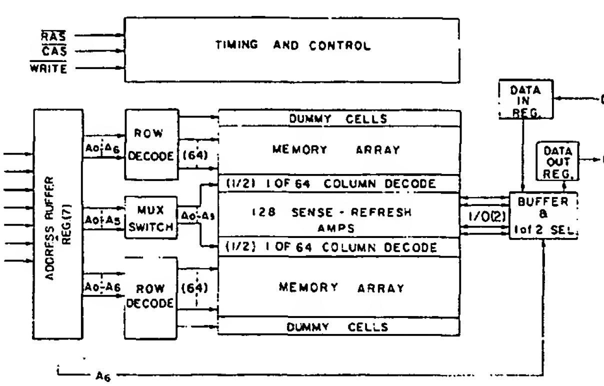

FIGURE 1 – Block diagram.

[1] *Electronics*, Vol. 48, No. 26, p. 29; December 25, 1975.

[2] Ahlquist, C.N., Breivogel, J.R., Koo, J.T., McCollum, J.L., Oldham, W.G., and Renninger, A.L., "A 16K Dynamic RAM", *ISSCC Digest of Technical Papers*, p. 128, 129; Feb., 1976.

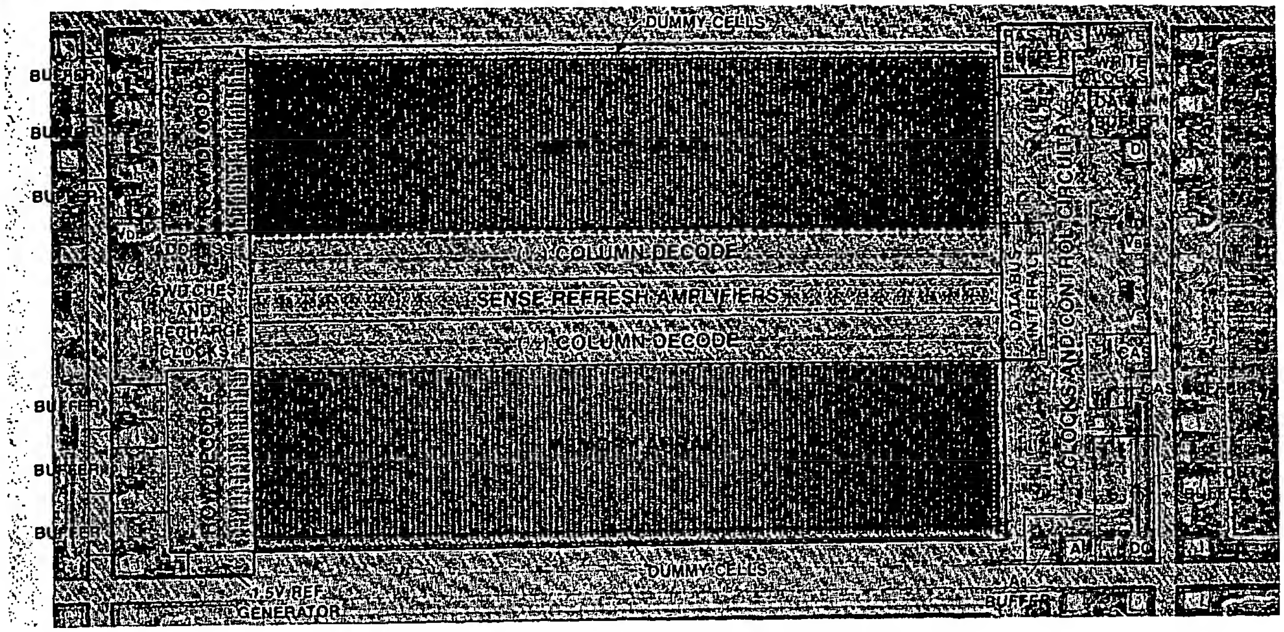

FIGURE 2 – Photograph of a 16K die showing location of important circuit blocks.

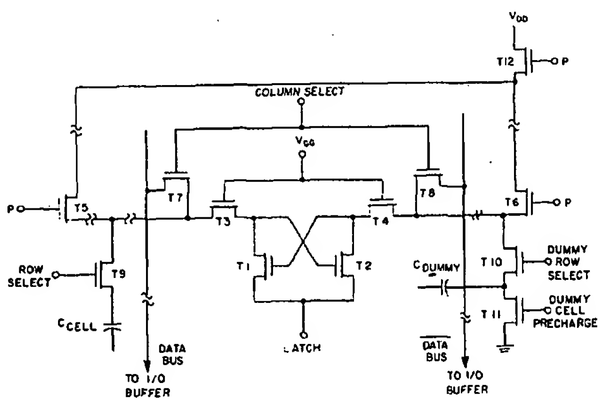

FIGURE 3 – Digit and sense circuit schematic.

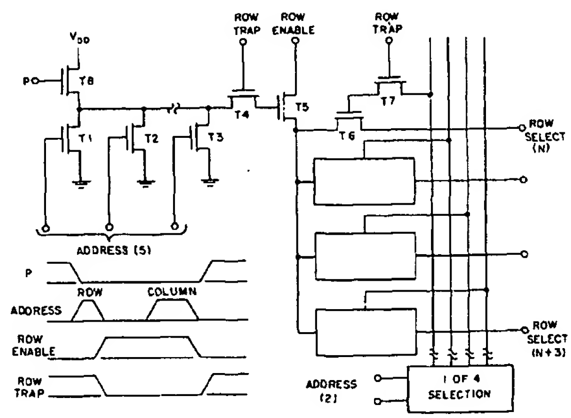

FIGURE 4 – Row decode circuit.

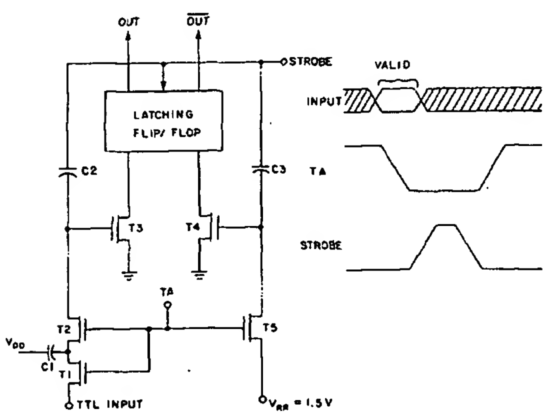

FIGURE 5 – Address buffer showing operation of input stage.

TECHNOLOGY	2 LEVEL POLY N SI GATE
CELL SIZE	0.7 MIL^2
DIE SIZE	0.122" x 0.227" (27,700 MIL^2)
ACCESS TIME	150 NS
CYCLE TIME	250 NS
SUPPLIES	+12, +5, -5 (ALL ±10% TOLER.)
ACTIVE IDD CURRENT	20 MA (@ 500 NS CYCLE)
STANDBY IDD CURRENT	0.8 MA
REFRESH	128 CYCLES/2 MS.

FIGURE 6 – Summary of typical characteristics of the 16K RAM.

SESSION II: FET Memory

WAM 2.2: A TTL Compatible 4096-Bit N-Channel RAM

R. Proebsting and R. Green

Mostek Corp.

Carrollton, Tex.

AN N-CHANNEL 4096-BIT dynamic MOS memory is being developed for both large and small memory applications. The primary design goal is to combine in one chip both ease of use and economy. To achieve ease of use, the usual requirement of external address latches, level converters, sense amplifiers and output latches have all been eliminated. The multiple high-level clock requirement has been replaced by a single low-level, low-capacitance input timing signal. System economy is achieved by both the inherent economy of a 4096-bit chip as well as the elimination of most of the support hardware normally required for largeMOS RAMs; Figure 1.

A 64 x 64 storage matrix uses one transistor and one capacitor per cell. The advantage of this cell over a three-transistor cell is its small size without sacrificing the yield loss associated with extremely tight geometries. The disadvantages are twofold. First, a relatively large storage capacitor is required in each cell. Second, even with a moderately large capacitor, the voltage applied to the internal digit bus is rather small – about 1 to 2 V – rather than the full digital voltage swing provided by athree-transistor cell.

To accomodate the first requirement of the one-transistor cell – a high storage capacitance – a special process was developed. One plate of the storage capacitor is simply an enlarged diffused source region of the transistor used in the cell. The other (grounded) plate of the storage capacitor is a deposited polysilicon layer which is physically located right under, but insulated from the decoded metal address line to achieve high functional density. Silicon nitride was chosen for the dielectric of the storage capacitors because of its low pinhole density, its high dielectric constant, and the fact that its use and technology are well established. The silicon nitride layer can be thin for high capacitance (0.6pF/mil^2), due to both the dense nature of nitride dielectric and by the non-reactive nature of the polysilicon above.

But even with moderately high capacitance per unit area, the requirement of 4096 storage cells puts an upper limit on both cell size and cell capacitance. The large stray capacitance of a digit bus with respect to that of a storage cell (4:1) attenuates severely the cell voltage seen by the sense amplifier. A logical *1* from a cell may only cause the digit bus to be one volt higher than that caused by a logic *0*.

To accommodate the low voltage difference between a *1* and a *0*, a new approach has been taken in the sense amplifier design; Figure 2. Rather than precharge the digit bus to precisely the switching threshold of an amplifier – a process requiring precharging for many RC time constants – the digit bus is precharged to a somewhat arbitrary voltage. This voltage is then sampled and held on a capacitor, the sampling taking place during and after the precharge of the digit bus, but terminating before a cell storage capacitor is addressed. When a cell storage capacitor is addressed, the digit bus comes to a new voltage level depending on the charge (information) stored on the storage cell. This new voltage and the previously-sampled reference voltage are then fed to a differential amplifier, the output of which drives the digit bus to restore data to the storage cell. The addressed sense amplifier also feeds its data to the output buffer.

The differential amplifier approach to the sense amp design provides two advantages over a single ended amplifier. First, the voltage to which the digit bus is precharged is not critical since it is a differential voltage that is amplified. This permits fast precharging of the digit bus without consuming a lot of power. Second, the differential amplifier is very tolerant of power supply voltage variation, permitting noise on the supply line during the critical time between precharge of the digit bus and amplification of the new voltage on the digit bus after cell access.

Dynamic MOS circuit techniques, which require multiple clock phases, are faster yet dissipate less power than do static techniques. To achieve high performance this circuit makes extensive use of well established dynamic techniques. But rather than put the burden of multiple phase clock generation on the user of the circuit, all high-level internal clocks are generated from a single TTL level input timing signal. Both the positive and negative edges of the input timing signal generate their respective internal clock sequences. The positive edge terminates an active cycle in proper sequence; turning off the selected decoder output line before starting to precharge the digit buses. It also prepares (precharges all modes to proper voltages) the entire circuit in readiness for a new active cycle.

The negative edge of the timing signal also generates a sequence of internal clocks. The first few clocks strobe, latch, buffer, and decode the address inputs while terminating the precharge in the proper sequence. Later clocks provide proper sequencing of the sense amplifier feedback, while the last clock activates the output buffer (if the chip is enabled). The output enable clock signal is unique in that one external timing signal edge causes two edges of this internal clock. The negative input edge causes the output buffer clock signal first to go off (open circuiting the output) and then to go back on (enabling the output with new data). Thus, the output data does not terminate with the beginning of precharge time, but remains valid through precharge time and disappears after a new cycle begins.

The best feature of the clock generator, in conjunction with the dynamic circuitry used in most of the remainder of the chip, is the low power consumption. Significant power is consumed only while internal voltage transitions are taking place. A few hundred nanoseconds after a negative input transition, or a hundred nanoseconds after a positive transition, total power consumption drops to a few mW. Thus, low standby power is achieved by gating the input timing signal with a chip select decoder. Unselected chips, receiving no

timing edges, dissipate only a few mW per bit. Selected chips dissipate power in direct proportion to frequency, this power being approximately 60 mW per bit at a cycle rate of 2.5 MHz.

The low active power, low standby power, economy, and high packing density of 4k packages make this circuit attractive for large memory applications. Also, due to the elimination of most of the support hardware usually required by large MOS memory systems resulting from internal clock generators, address latches, level converters, sense amplifiers and output buffers all on the chip, the circuit can be used for small as well as large memory systems.

Technology:	Modified N channel self-aligned metal gate
Chip Size:	156 x 184
Cell Size:	2.3 mil^2
Organization:	4096 words by 1 bit
Input levels including clock:	$0 \leqslant .8$V; $1 \geqslant 2.4$V
Output:	Push-pull-open < 200 Ω to Gnd or to +5V supply
Read access time:	< 300 ns
Read cycle time:	< 400 ns
Write cycle time:	< 400 ns
Read/Modify/Write cycle time:	< 500 ns + modify time
Standby power:	< 2.5 μ W/bit
Active power @ 2.5 MHz:	< 60 μ W/bit
Power supplies:	+12 V, +5 V, -12 V, Gnd
Refresh:	64 cycles required each 4 ms

TABLE 1 — Device Characteristics

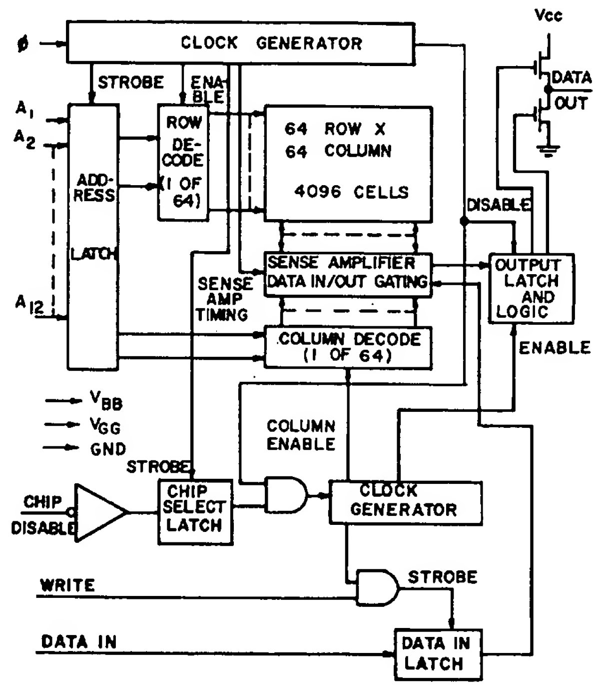

FIGURE 1—Block diagram of 4096-bit RAM.

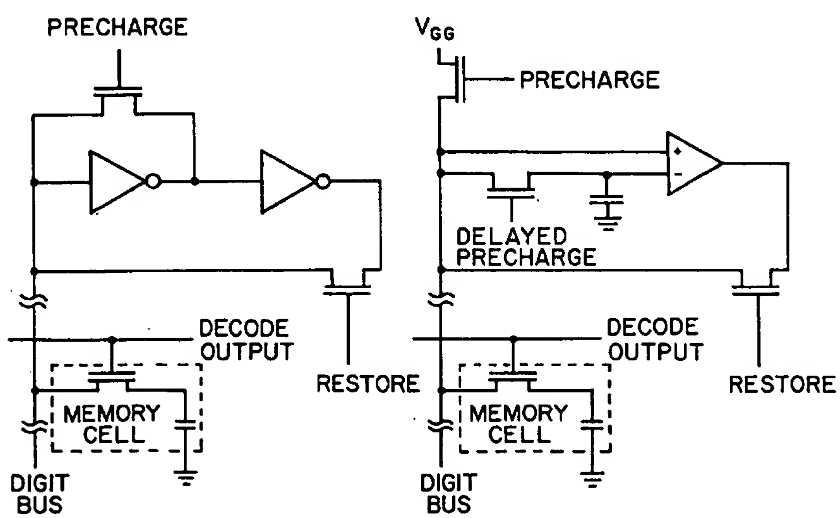

FIGURE 2—Sense amplifier technique.

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1 **Video-rate pyramid optical flow computation on the linear SIMD array IVIP**
Johannesson, M.; Gokstorp, M.;
Computer Architectures for Machine Perception, 1995. Proceedings. CAMP '95 , 18-20 Sept. 1995
Pages:280 - 287

[Abstract] [PDF Full-Text (540 KB)] **IEEE CNF**

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2 **High-throughput VLSI architectures for the 1-D and 2-D discrete cosine transforms**
Chin-Liang Wang; Chang-Yu Chen;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 5 , Issue: 1 , Feb. 1995
Pages:31 - 40

[Abstract] [PDF Full-Text (784 KB)] **IEEE JNL**

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3 **New systolic array implementation of the 2-D discrete cosine transform and its inverse**
Yu-Tai Chang; Chin-Liang Wang;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 5 , Issue: 2 , April 1995
Pages:150 - 157

[Abstract] [PDF Full-Text (640 KB)] **IEEE JNL**

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4 **A data-flow processor for real-time low-level image processing**
Quenot, G.; Zavidovique, B.;
Euro ASIC '91 , 27-31 May 1991
Pages:92 - 95

[Abstract] [PDF Full-Text (276 KB)] **IEEE CNF**

5 **Computer-aided synthesis of a bi-dimensional discrete cosine transform chip**
Rampa, V.; De Micheli, G.;
Circuits and Systems, 1989., IEEE International Symposium on , 8-11 May 1989
Pages:220 - 225 vol.1

[Abstract] [PDF Full-Text (332 KB)] **IEEE CNF**

6 **A mixed-signal VLSI neuroprocessor for image restoration**
Lee, J.-C.; Sheu, B.J.; Choi, J.; Chellappa, R.;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 2 , Issue: 3 , Sept. 1992
Pages:319 - 324

[Abstract] [PDF Full-Text (516 KB)] **IEEE JNL**

7 **Systolic realisation for 2-D convolution using configurable functional method in VLSI parallel array designs**
Che Wengang; Li Yanda; Jiao Yue;
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Pages:361 - 367

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8 **New architecture for high throughput-rate real-time 2-D DCT and the VLSI design**
Jen-Shiun Chiang; Hsiang-Chou Huang;
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Pages:219 - 222

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9 **High speed and continuous 3-D measurement system**
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[Abstract] [PDF Full-Text (380 KB)] **IEEE CNF**

A Single Chip Video Signal Processing Architecture for Image Processing, Coding, and Computer Vision

John Goodenough, Richard J. Meacham, Jonathan D. Morris, N. Luke Seed, and Peter A. Ivey, *Member, IEEE*

***Abstract*— A new VLSI architecture for an internally multiprocessing, single chip, SIMD-based Video Signal Processor (VSP) is presented. The limitations of extended DSP architectures and conventional Array Processors are discussed in the context of image processing, coding and computer vision. How this gives rise to the architecture is described. Architectural flexibility is provided by the integration of a novel array-based processing core, together with a RISC Processor, Intelligent Memory Interface Processor, and internal cache RAM. The array core architecture is a second generation, enhanced array whose key features are: 2 b datapath, dual processor mesh-connected array planes and combined SIMD/Systolic functionality. The core is optimized for 2-D windowed operations, particularly 2-D multiply-accumulation and transforms. The device is expected to operate at 80 MHz on low voltage silicon and deliver real-time performance across a range of target applications**

I. Introduction

THE growing market for multimedia and computer vision has generated a great deal of interest in VSP solutions [1]. We propose a VSP which is intended to provide general microprocessor functionality for control and system-level activities while explicitly accelerating the primitive core operations related to 2-D signal processing. We anticipate that such a device will find wide application due to its flexibility.

Both multimedia and computer vision are characterized by relatively fluid algorithms: In the case of multimedia, the march from H.261 through MPEG-I and II toward object-based coding methods for very low bandwidth proceeds apace. There is, consequently, a clear demand for devices which can address the raw performance requirements of these tasks while providing the end user with a high degree of flexibility for integration into different applications. In the computer vision domain the underlying functions are well explored, but the way in which processes are linked together to provide robust implementations for object recognition, 3-D stereo, and motion tracking is the subject of great research interest [2]. A device which accelerates the primitive operations in both these areas may facilitate more rapid development of new algorithms and solutions.

Recent activity toward this goal has been based on extensions of conventional DSP architectures. Performance through increased clock speed has been pursued by many; for example the 300 MHz device in [3]. Such approaches produce large chips with high power consumption which still fail to deliver competitive levels of performance. Other workers have implemented a parallel pipelined approach [4], [5] or used a mix of dedicated functional blocks [6]. We outline in the following sections why we believe these approaches result in inefficient use of silicon.

Our approach stems from traditional SIMD Array Processors, whose lineage stretches back to MPP and DAP through more recent implementations such as Blitzen [7]. This work extends our earlier success with such architectures: At wafer scale in the ELSA program [8]; and a first generation integrated array based processor, the DIP chip [9]. We focus on and optimize the more traditional array-based approach taken in these implementations by the integration of a RISC processor macrocell; Intelligent Memory Interface processor and its associated cache memory; and application specific processors. These features, in conjunction with careful core-datapath design, improve silicon performance, increase flexibility, and ameliorate the IO bottleneck traditionally associated with Array Processors. Our goal is to produce a flexible architecture which addresses the mandatory performance requirements of H.261 and MPEG-I with a competitive silicon budget while providing the ability to address a broader range of application domains.

II. System Architecture

A. System Integration Issues

Whatever the architecture and performance of a core signal processing engine, it must be carefully integrated with support components in such a way that it yields a credible system component. In particular the design must not devolve the problem or costs of access to image data structures to the system designer; for example, requiring large amounts of high cost, high power SRAM, or complex external data multiplexing schemes. Similarly, the device must not require a large pin count which contributes excessively to component and, hence, system cost.

We believe that a majority of the VSP's developed hitherto have failed to address either or both of these constraints [10]. We, therefore, fixed system constraints prior to architectural specification, limiting ourselves to the use of commodity DRAM's for external data store and hence opting to rely on in-

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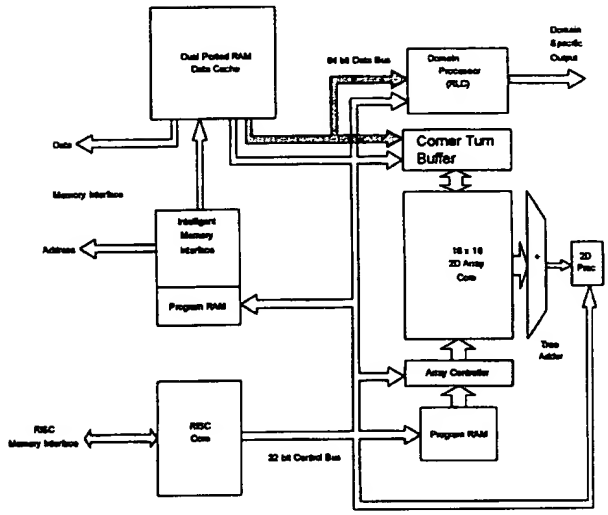

Fig. 1. Top level VSP architecture.

ternal cache and memory management to achieve performance. In addition, we set a maximum pin count of 169, including power. This latter constraint immediately removes the ability to support multiple image data ports, but as we will show this is not a limiting factor for most applications.

Our chosen design and implementation methodology consciously mirrored our goal of performance and flexibility by capitalizing on the advantages of structured semicustom gate arrays. We combined full custom macroblocks for the signal processing core together with generated memories. In addition we synthesized gate-array for control functions and for domain specific processors.

Clearly gate-array offers considerable design-time reductions for the implementation of small, modest-performance, domain specific processors. As an example of this, consider a coding application which requires a run length coder. This can be rapidly generated using standard synthesis techniques and then integrated together with the full custom macroblocks. Furthermore, we recognized the progress made in the implementation of microprocessor cores and have chosen to develop the architecture to permit any standard 32 b microprocessor macrocell to be integrated on chip. For our prototype we selected the ARM6, due to its high power efficiency (MIPS/W), which is in keeping with our overall low power objectives.

III. Top Level Architecture

The top level architecture is illustrated in Fig. 1. It is designed to support the processing of images or image regions as abstract data types—it is intended that all image or pixel registered operations are performed, where possible, on the VSP core. It is such operations which are frequently the bottleneck for more conventional processor architectures.

The signal processing array core deals with image regions as "objects" and returns results either as new pixel registered "objects" or as single extracted values—for example, an average greyscale value. A significant problem with such an approach is that it does not always maximize performance in the presence of real-time data flow, since control of the array core (i.e., instructions) must be issued for each image patch object. To tackle this problem we have moved from a tightly coupled model (adopted in our work on the DIP chip which integrated a RISC engine [9]) to a loosely-coupled approach which is more in line with the requirements of real-time image dataflow.

In this scheme, the "objects" being processed on the core become sequences of image regions or patches. This enables, for example, an entire image to be filtered with a single "instruction." An "instruction" in this context is two small programs: One for the array, the second for the Intelligent Memory Interface (IMI). The IMI ensures that image patches are delivered to the Array core and returned to memory in parallel with the processing of the patches themselves. At the architectural level the IMI decouples the array core from external image data stores and ensures that it can achieve its maximum computational performance through data caching—this is discussed in more detail in Section VII. These programs are loaded into the respective processors' local memory (setup); each processor is then activated (execute), and proceeds to perform its operation independently of the RISC Processor. Sequencing is controlled by data interlock between the IMI and Array core. Thus, if the array core requires data, it will wait until the IMI has delivered that data to it before continuing. However, both will work in parallel.

All of the functional processors operate using a communicating sequential process (CSP) paradigm. This enables images (or other 2- and 3-D data structures) to be processed as far as possible in a dataflow mode with a minimum of control and synchronization latency. Thus, the RISC Processor is released from housekeeping work, freeing it for tasks involving conditional execution of results computed in the array core, or to perform high level algorithms consistent with the requirements of image understanding [11] and overall system control. Note that the RISC has full access to all image data whether in external RAM or internal cache RAM and is, therefore, as flexible as any conventional microprocessor. Furthermore, the RISC can control each functional block directly if necessary.

Data Load and Unload operations to the array core are carried out by shifting data between an on-chip, dual ported, cache memory (DPRAM) and the Array core via a Corner Turn Buffer (CTB). The CTB is basically a dual ported parallel-serial register moving between byte- or word aligned data and the nibblet-serial representation used on the array itself. An independent internal 64 b data bus exists for rapid data transfer from cache to array core via the CTB. A complex data mapping scheme enables data to be transferred to the CTB from the DPRAM in a single cycle. This operates irrespective of data alignment and significantly reduces data transfer latencies.

IV. Core Signal Processor Design

The design of a core signal processing engine which gives performance and flexibility with high silicon utilization is crucial to the success of the device. From a programmer's perspective this can be viewed rather like the addition of a dedicated floating point accelerator in a conventional microprocessor. We selected an Array Processor for the following reasons:

1) An Array Processor gives massive parallelism which inherently capitalizes on image data structures. With current technology, however, this can only be implemented using small processing elements. A survey of applications revealed this to be an advantage with respect to silicon utilization due to the wide range of bit lengths encountered in data representations of pixels, coefficient masks, and intermediate results. For example, a simple filter may use 2-b coefficients and 8-b pixels; an H.261 DCT requires 14 b coefficients; video standards commonly use 10 b pixels, etc.

   However, while many coding and filtering applications are well defined, practical computer vision applications tend to be particularly difficult since they pipeline several steps together and data accuracy must often be maintained at intermediate stages. For example, in the Harris/Stephens corner detector [12] the required bit accuracy grows from 10–36 b. A bit-or nibblet-serial processor will have a higher utilization than a corresponding pipeline element (which must be sized for the maximum expected word width).

   Consider a 10 by 4 b multiply (common in filter operations). On a 16 × 16 multiplier a large percentage of the silicon is inactive for much of the time. Performing the multiplication serially results in all of the silicon being used for exactly the required number of clock cycles (this minimizes the generic area-time product). Note that several proposals have been made to segment large multipliers into chunks, for example in the MVP [5], but there is a hidden mapping problem in their optimal use, since data must be explicitly packed into memory store, having been quantized into the appropriate segment lengths.
2) Many applications in image processing exhibit locality of reference for an individual operation *and* between successive operations of the same type (i.e., in both the spatial and temporal domains).

   Consider a filter mask moving over an image; successive applications of the mask use largely the same data—only one new row or column from the image is required at the point of computation. Using a mesh connected array architecture enables data already *local* to the array to be shifted to nearest neighbor processors limiting the off-array data transfer to a single new row/column. Contrast this with the basic DSP multipipeline where all data (coefficient and image) must be re-fetched from memory for each invocation of the kernel unless local FIFO's are employed to serve this need.

   Thus, an array based approach leads to reduced on-chip, core to memory data bandwidths for a range of critical algorithms and hence aids lower power operation. In many large microprocessor and DSP designs, long multiple busses (often implementing crosspoint connection schemes) connect pipeline processing elements to memory. These contribute greatly to capacitive load and hence power dissipation in addition to limiting the machine cycle time.

   It may be argued that in an array-based design one merely exchanges the data transfer problem for one of numerous control lines. However, in our analysis of the control line activity for such a design we found that over a wide range of algorithms they change state relatively infrequently. Thus the effective switching capacitance involved is lower than might be expected. This factor, coupled with the decreased switching capacitance associated with data transfer yields a low power dissipation.
3) A multipipeline, despite providing a more accessible computing paradigm, devolves the responsibility for achieving performance to the user. In this context, general purpose compilers are of little help since the data mapping is domain dependent. Each pipeline requires access to independent (either separate or through multi-porting) RAM blocks. The user can be presented with a bewildering set of alternative mappings. Data structures must be distributed across memories in such a way that zero contention access is guaranteed if performance is to be maintained and the computational core not stalled.

   In contrast, an array has only a single homogeneous cache memory and a defined 1- or 2-D block data structure. This is clearly appropriate for windowed filters, block or whole-image correlations, temporal filters (where successive frames can be overlaid) and transforms via block radix methods [13]. The fixed structure removes many of the degrees of freedom and so simplifies the programming task.
4) A final motivation for an array is in the implementation domain. The regular layout enables considerable optimization of the basic processing element (PE) element to be carried out—it can then be replicated with relative ease. The net result is that a very large custom macrocell (~1 M transistors in this case) can be implemented with a greatly reduced design effort. This can be contrasted with a block based approach where independent functional units must each be hand crafted. The commercial advent of >2 layers of metal interconnect has increased the viability of the array architecture since it is now possible to utilize metal interconnect within individual PE's and to increase control line density enabling more useful local memory architectures to be practically conceived.

V. Array Core Architecture

The array core is illustrated in Figs. 2 and 3 and it is a mesh connected architecture. The size of the array core processor is 16 × 16 PE's. The motivation for this choice is twofold: It is the correlation block size commonly encountered in coding applications, and it encompasses the largest filter mask size commonly used in image processing (this being a 15 × 15 Difference of Gaussians).

We recognize that many applications operate on 8 × 8 blocks or smaller. The array core can, therefore, be partitioned into four 8 × 8 quadrants. This enables, for example, four 8 × 8 DCT's to be simultaneously computed. Larger blocks can be spatially decomposed and smaller mask sizes, for example those involved in image filtering, can be tackled by embedding multiple instances within the array simultaneously. Thus, 25

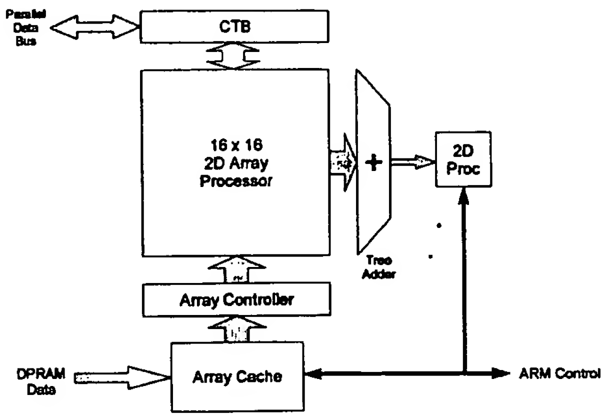

Fig. 2. Core signal processor and CTB.

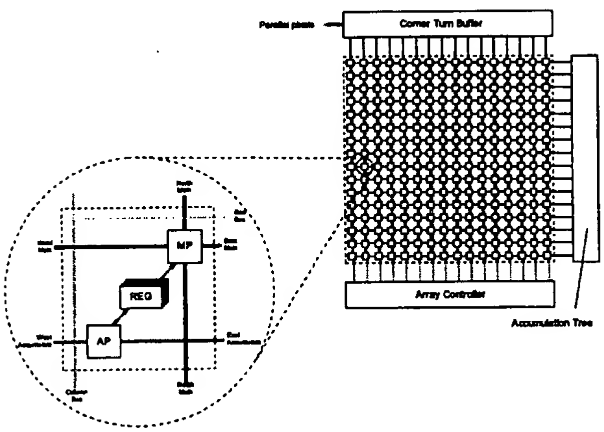

Fig. 3. Array architecture with PE detail.

3 × 3 filter kernels can be independently computed on a 15 × 15 pixel window. The fact that these kernels are congruent with respect to the image leads to very low image IO data rates between filter applications.

While recognizing the suitability of the array approach we have addressed several shortcomings and added enhancements compared to more standard SIMD array architectures. The basic operation underlying many high level functions involving images is a 2-D windowed *operate-accumulate* operation (usually multiply-accumulate in computer vision or the mean absolute difference—MAD—in coding). Standard SIMD approaches yield rapid operate phases, all PE's running in parallel, but give poor speed up and PE utilization during a separate accumulation phase, when the amount of concurrent computation is greatly reduced. For example, in the final stage of a 2-D accumulation only a single column of the array is active. By adding the capability of systolic addressing which was first used in our first generation device, the DIP chip [9], the situation is dramatically improved.

We go beyond this, by the innovation of adopting an internally parallel PE within the array, which supports concurrent 1-D *accumulate* operations during the next *operate* cycle. To accommodate full 2-D accumulation, while maintaining maximum utilization, it is necessary to introduce a nibble serial tree adder as shown in Fig. 2 on the East side of the array. This adder accepts the 16 partial accumulations produced from each row of the array and combines them to produced a final result. The result is fed into an independent functional block termed the 2-D Processor (2-DP). This block performs computation on the resulting accumulated values, for example normalization or comparison to a pre-stored value. By providing the tree adder and independent 2-DP we remove an enormous overhead from the RISC both in terms of computation and synchronization while improving the utilization of the array core.

We were also concerned about the ratio of computational resources to memory resources within conventional, one-bit SIMD PE's, considering it to be too low, particularly for compute-intensive operations like multiplication. With bit-serial architectures, multiplication is performed by repeated shifted additions: With a two-bit PE this requires half the number of clock cycles to execute. In many cases, the size of the local registers is fixed by the applications being considered and is relatively independent of the datapath. Moving to a 2 b datapath, with the same amount of local RAM, offers a speed-up of nearly 100% for all such operations. This speed-up incurs only a relatively small increase in critical path delay (dominated by increased interconnect delay within the PE itself rather than the ALU delay). The majority of a single (two bit operation) cycle time is spent in issuing a new address (including the significant skew of the address lines themselves) and routing the data to and from the ALU though multiplexors. The PE datapath area is roughly doubled in size, but this only contributes an extra 25% to the total PE area when power bussing, local RAM and nonlocal interconnect are considered. Thus the move to a *nibblet-serial* processor involves only a modest increase in the resultant chip area but yields a computational speed-up of nearly 100%. It should be noted that the use of two bits is only minimally wasteful when extended to multibit arithmetic.

The basic element of the array core is the 2-b, dual-processor PE (shown in Fig. 3). The main processor, MP, is mesh-connected to its nearest neighbors and supports a full range of arithmetic and logical operations, including implicit (no overhead) support for signed arithmetic. Local flag operations allow conditional data selection (in image comparison or clipping operations, for example). Each PE is equipped with the ability to perform conditional operation/no-operation and to support in-line programming of constants.

Four 32-b local registers provide the data store, two of which are shared with the independent Accumulation Processor (AP) providing the mechanism for data exchange between the two. The AP operates in one of two modes. It exists as an independent mesh connected plane for data shifting operations or operates as a systolic array of nibblet-serial pipelines for accumulating partial products from West to East along the rows of the array. The accumulation plane is connected to the nibblet serial adder tree for full 2-D accumulation. The 2-D tree adder and processor are generated in synthesized gate array and it is possible to rapidly customize this final processing stage.

The array core is also spanned by row and column buses, which are interconnected along the leading diagonal of the array. These buses enable row/column data transposition operations between PE's without shifting data off to a nonlocal transposition memory. This feature supports accelerated trans-

form kernels for DCT, etc., and allows data to be loaded or unloaded from any location within the array without being shifted through intermediate processors. It also facilitates the broadcast of common coefficients to all PE's within a row or column simultaneously. The ability to load data via the bus structure enables the computational window defined by the array to be arbitrarily moved in any direction through a large field of data. This feature directly supports directed correlation schemes encountered in coding or stereo correspondence algorithms [14].

VI. Core Control Architecture and Instruction Set

The array controller and instruction are designed to provide maximum user flexibility while removing a major drawback of many Array Processors—that of the demand instruction bandwidth required to prevent the Array from stalling. Given a two bit processing element, many operations will be identical for a number of cycles. For example, an 8-b addition retains the same basic datapath configuration for four array clock cycles. Furthermore, analysis of the datapath reveals that many operations have some difference in the final cycle of an operation—for example clearing the carry or latching a conditional flag.

At the basic level, all core instructions therefore consist of four primitive fields:

1) ⟨datapath_configuration⟩
2) ⟨final_cycle_configuration⟩
3) ⟨address_offsets⟩
4) ⟨nibblecount⟩.

Into this class fall all the basic arithmetic and bitwise logical operations. Depending on the data operands, these microinstructions trigger CTB address generation to load data onto the array. Should the CTB not be ready, the microinstruction engines will stall until data is present, hence supporting the CSP model described in Section III.

Abstracting further, many instructions are repetitions of the basic instructions (for example, multiplication which is implemented through shifted addition, with appropriate sign extensions), or themselves repeat in a regular fashion—for example, a 1-D transform containing repeated multiplications. The array controller, therefore, supports three levels of looping, minimizing the macroinstruction rate at its input. The hardware loop counters can be accessed explicitly through set-count commands or can be implicitly set up during specified complex instructions. The decode and control circuit is entirely synthesized so it is relatively easy to introduce new complex instructions, following evaluation, for a production chip. This would reduce the amount of store required and in many cases would enable a small on-chip ROM to provide the instruction store. Additional counters are provided to enable software looping and these have support for variable radix increment and decrement as required for large transforms, or directed block matching schemes. The controller pipeline is shown in Fig. 4.

The first pipeline stage is an instruction expander and data reordering queue which extracts variable length instruction words from the input data stream. This unit also determines

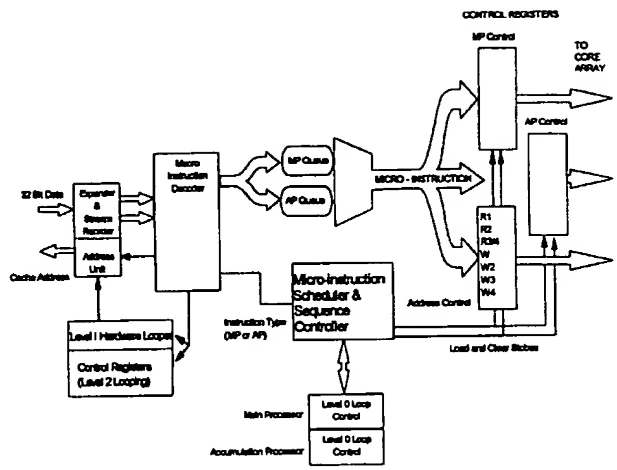

Fig. 4. Array controller instruction pipeline.

look-ahead addressing for branch and loop operations.

The second stage macroinstruction decoder passes microinstructions onto the sequencing engine. It also locally decodes flow control and level 1 hardware looping operations. The decoded microinstructions are passed to the microscheduler which demultiplexes them into one of two register/counter primitive control engines (depending on whether the instruction is destined for the main or accumulation processor). Each of these microcontrollers is double buffered. This replication minimizes latency between microinstruction operations.

During microinstructions, address incrementing for the array core's registers is simply controlled via shift registers. This will enable very high speed operation to be supported in the future. Synchronization tokens may be attached to any microinstruction, destined for either the main or accumulation processor. The microscheduler then holds the first arriving instruction in a hold register until the corresponding synchronized instruction for the other engine appears. They are then loaded onto the array control registers simultaneously. In this way, fork operations can be tightly controlled in the microinstruction stream to ensure data coherency. The microscheduler can also prevent any microinstruction clashes where both the MP and AP attempt to use the same PE resources.

VII. Intelligent Memory Interface and Data Transfer Subsystem

Overcoming the data transfer bandwidth is an important aspect of any VSP design. Operations must be carefully overlapped, balanced and sequenced to ensure that the most efficient use is made of the external memory interface without starving the signal processing core of data.

Two operation modes are available to transfer data between the CTB and Array core. In the first mode, the row/column bus structure previously described enables any individual row or column to be accessed. The second mode writes directly to the periphery of the array, data being shifted down between processors. This second mode is one feature which reduces power consumption since all transfers are local and the global busses, representing a significant capacitive load, are inactive.

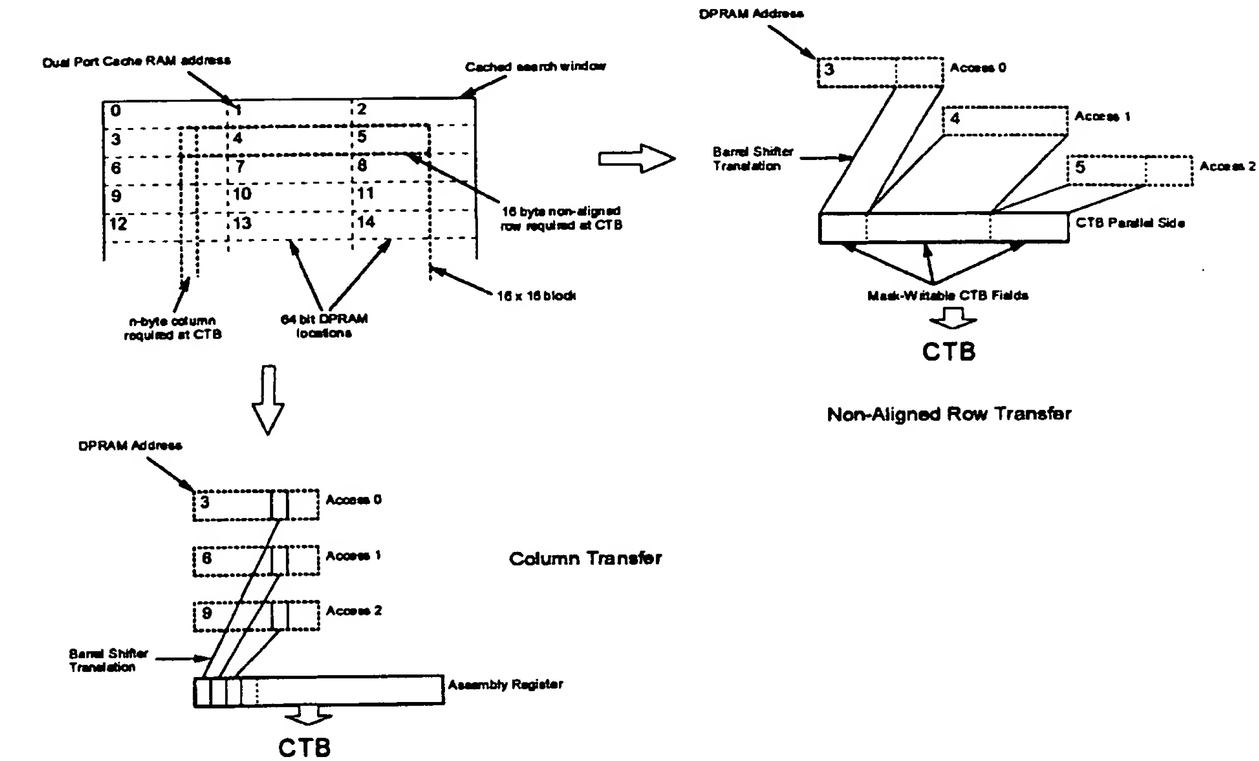

Fig. 5. Cache RAM special access modes.

Algorithms can be structured so that load balancing between main and accumulation processors maximizes the available parallelism (recall that both are capable of shifting data). This approach contrasts with that taken in our earlier work, where each PE had double buffered register memories locally. We adopted a new approach for a number of reasons: Firstly the impact on PE area due to the register duplication; the overhead of the independent IO to these RAM's, particularly in terms of package pin count and the multiple CTB's required to support data transfer. Each CTB occupies the equivalent area of one row of PE's and therefore contributes greatly to the total chip area.

Examination of the expected modes of operation with respect to data transfer indicates that multiple IO busses would lie idle for a large portion of the time. In fact the only operations which benefit from multiple busses are those very simple operators which we term pixel point operators (such as a simple image addition). These are characterized by a low number of dynamic computational steps per pixel. Many coding and computer vision algorithms do not perform simple operations in isolation which can be usefully concatenated with other stages, thus changing the balance between computation and IO.

The peak data demand to the array (in excess of 300 Mbyte s^{-1}) is only encountered during the primary load phases and, providing the internal cache holds the required data, this can be met as described below. The data transfer bus is only subsequently used in bursts to update new rows or columns. In order to avoid unnecessary latencies the CTB incorporates a wide fan-out multiplexor which is capable of loading all CTB locations in two cycles. A 64 b internal bus connects the CTB to the DPRAM, and a relatively modest 40 MHz bus cycle time is then sufficient to meet the peak data demand when data is shifted onto the array.

In many image processing applications we are faced with a problem of accessing pixel data from information stored in wide word memories—the wide word storage being necessary to satisfy data bandwidth requirements. Many systems duck this issue or leave it to the board level design to solve. In our architecture the data transfer path from cache to array features a byte ordered barrel shifter enabling data within the DPRAM to be accessed *across* 64 b word boundaries. This enables arbitrary, pixel oriented, data windows to be accessed.

A similar challenge is often encountered in accessing "columns" of image data which are spread across different wide word locations. These access modes are diagramatically represented for an arbitrary 2-D image region held in the DPRAM in Fig. 5. The intelligent memory interface (IMI) solves both these problems and gives the capability to provide concurrent access between external memory and cache while performing internal transfers between DPRAM and Array core. Access to image data structures not stored on wide word-width boundaries is carried out by a background process which pre-assembles columns or slices of data into an assembly register. This parallelism ensures that transfer to the CTB and Array is achieved, on demand, with minimum latency. This process takes advantage of the bursty, and often predictable, nature of the demand from the array core itself.

The IMI, shown in Fig. 6, supports a sophisticated command queue enabling the controlling RISC to pass command

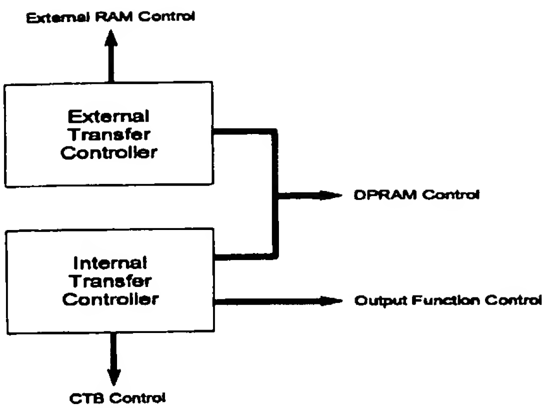

Fig. 6. IMI block diagram.

sequences of up to 128 commands to the IMI which will then perform complex external to internal transfers without further intervention. The IMI internally interlocks the delivery of data blocks with other activities within the device to ensure coherency between data stored in external memory and that transferred to the array core. Complex data scanning patterns such as a "snake" scan through a 2-D region are supported in a single instruction. A direct link to the 2-DP is provided to support block address indirection. The block number of, for example, a matched macroblock in a particular sequence can be supplied to the IMI from the 2-DP, which will then perform a block load from the supplied address. This feature closes one of the most time-consuming control overhead loops in the implementation of conditional algorithms.

The IMI provides a seamless interface to commodity DRAM or VRAM, reducing system cost and power consumption. Page mode access enables a peak bandwidth of 100 Mbytes·s^{-1} to be delivered. It is important to remember that any chip operates "in-system" and that for very simple operations (e.g., image addition) the limiting factor will always be the external data interface. The array core approach provides performance advantage where data is reused between successive operations.

VIII. User Programming Model

The array core possesses its own assembler, and it is fully programmable, including single step debugging. However, it expected that most users would use precompiled library calls for common functions. The macroinstruction sequencer for the array permits branch and jump instructions within its memory space. A pseudocode compiler based around the Occam language is being developed to control the parallel operation of the separate threads in the device; those of the Intelligent Memory Interface, Array, and Domain-specific functional blocks. This language captures the dependencies of the dataflow and is consistent with the hardware interlocks which implement the CSP model. In terms of implementation, this allows the RISC to set up all of the internal functional blocks and the sequence of their operation is determined by the availability of data at each stage. That is, the CTB will not fill the array until the data has arrived from the cache under control of the IMI. We anticipate that for demanding routines and applications the "cache →core →result register" datapath will operate in a "setup and execute mode," where each component operates in a data-driven style.

Currently, both the Array and IMI are initiated by writing control programs into their local address space, followed by an initial instruction pointer which commences execution. This feature enables the next code fragment to be preassembled in local memory prior to operation. A future device will incorporate the additional ability for both units to autonomously access external program memory. Global conditional operations rely on the RISC, or other controller, processing data derived from the array itself (either blocks in the internal cache memory or results from the 2-DP) and switching address and/or instruction pointers for the memory control engine and core signal processor to allow data dependent operation.

IX. Example Application

In this section, we outline the way in which the device can be used to tackle aspects of real-time image coding algorithms. This will give the reader an appreciation of the interaction between the functional blocks. The examples given form part of the macroblock processing aspects of the MPEG coding algorithm [15]. In performing such algorithms it is intended that, wherever possible, the array operates in conjunction with the IMI and independently of the RISC engine. In practice, the RISC engine will have little to do apart from setting up each of the major functional blocks. The array is responsible for performing the DCT, IDCT, Quantization, Motion Estimation. The 2-DP is responsible for finding motion vectors, and the Domain Specific Processor (RLC) is responsible for run-length encoding the data and delivering the data to an external entropy encoder (this function could have been designed into the Domain Specific Processor, but the choice of an external encoder was determined by the availability of existing devices). Data is transferred between functional blocks under the control of the IMI and command sequences (local to each functional block) ensure that all of the activities are coordinated.

A. Motion Estimation

Motion estimation is often implemented as a 16 × 16 block correlation between an area of the current input luminance image and a limited search region of a previous (or subsequent) decoded luminance image. The IMI is responsible for bringing both the candidate block and the search area from external memory into the DPRAM. The array core can accommodate many different search strategies: For example: Full, spiral, logarithmic, directed, or sparse [14]. The computation performed on the array core will, of course, vary depending on both the search strategy chosen and the terminal condition for each (i.e., whether a search would proceed only until an acceptable match is achieved, rather than being exhaustive with respect to the specific scheme being followed). We describe below the mechanisms to support these operations.

For a motion estimation algorithm the reference macroblock is loaded into one register ($R1$) of the array core. The first 16 × 16 candidate region from the search window is similarly loaded into a second register ($R2$). An absolute difference

matrix is now computed on the Main Processor (MP) of each PE, the result being placed in register ($R3$). At this point the multiprocessing capabilities of the PE are brought into use: The result of the first absolute difference is accumulated using the dedicated Accumulation Processor (AP). This results in 16 partial sums being produced, nibblet-serially, out of the East side of the array, accumulated, and passed to the 2-DP.

In parallel with this accumulation operation, the MP loads new data into $R2$ and performs the next absolute difference operation, placing the results in register $R4$. Further block match operations proceed with registers $R3$ and $R4$ acting as shared memory to transfer the results of the absolute difference operation between the MP and AP.

The time taken to load new data between successive matches depends upon the search strategy. Wherever possible, data on the array core is re-used, new data being shifted into position. For an exhaustive search, each new match operation therefore requires only a single row or column to be shifted onto the array. One further advantage of an array based approach to motion estimation is that half pixel interpolation can be performed locally by averaging pixel values between neighboring PE's, this further extends the potential search strategies which can be followed.

While the array itself is performing the concurrent absolute difference/partial accumulation, the tree adder completes the full 2-D accumulation and passes the result onto the 2-DP block. This result represents the match score of the current block, and is processed in the 2-DP to determine the block-match with minimum error. The 2-DP can be programmed to process either a specific number match scores (this number being determined by the search strategy) or to process match scores until a pre-determined condition is met. If, for a particular strategy, an acceptable match is found before an entire search pattern is complete, the looping operation of both the array and IMI is terminated on a signal from the 2-DP. Both then proceed to the next phase of the operation. Note that both array and IMI can execute jumps conditional on the 2-DP.

The next instruction, following a successful block match, waiting to execute on the IMI is *load block at pointer.* This pointer is computed from the block index for the best match stored in the 2-DP. This region can then be directly loaded onto the array for subsequent processing.

In order to further accelerate performance, the scenario described above is, in practice, more complex. Instead of processing a macroblock immediately that a best match has been computed, the block index is stored in the 2-DP. This enables a second motion estimation operation to be launched immediately the first has completed. During the computation of this second, independent motion estimation operation, the latencies of pointer retrieval and access of the chrominance data for the matched blocks are absorbed. The chrominance information from two successive macroblocks can be processed (DCT and quantization) at the same time.

B. DCT

A DCT operation is performed in-situ on the array core using a row-column decomposition technique—transposition between phases being internal to the Array core itself.

During the DCT operation, the 16×16 array is segmented into four 8×8 quadrants. DCT Coefficients are broadcast, using the column bus, so that all PE's in a given column receive the same coefficient. Multiplication by the broadcast coefficients takes place in each PE of the array simultaneously, thereby computing a set of partial products. Since the array core is operating nibblet serially it can support a variety of intermediate bit accuracies, as well as rounding, truncation and saturation techniques, as required by a particular algorithm. Once again the MP and AP are operated concurrently, the data being multiplied by the next set of coefficients while the current partial products are accumulated in the AP to provide a single filter tap result for the first pass (1-D) DCT. Note that with the array segmented into quadrants 32, 8 point 1-D DCT's are being computed concurrently. The resulting filter tap, accumulated on the East side of each 8×8 block, is immediately transposed using the row and column bus. Thus, after 8 1-D DCT's have been performed the data is already in the correct spatial arrangement to apply a second DCT pass. Identical processing to that described produces the final DCT results correctly registered on the array in a form suitable for subsequent quantization and output to bitstream post-processor as required. In our prototype architecture we have implemented a run length coder (RLC) as proof of concept. This takes data directly from the array core and re-orders it following a zig-zag scan, prior to entropy encoding. Output from this domain specific processor is via an independent output port.

We have seen that the array core and IMI operate in an independent fashion for such operations and this enables the RISC processor to effect control of the entire coding process. Typically in many applications, feedback from the bitstream coding is used to alter the performance of the macroblock processing. The RISC can direct the IMI to pass a different set of quantization parameters to the array as determined by the required codec characteristics. Alternatively, the RISC has access to all of the control registers associated with the 2-DP and the parameters associated with the match process itself can easily be altered.

X. Implementation and Performance

A device with the architecture described is scheduled for fabrication using a structured gate-array implementation on a 0.7 μm TLM low voltage process. The array core, memories, and CTB are highly optimized full custom blocks (designed to scaleable rules) while the controllers and memory interface use gate-array derived from logic synthesis.

Extensive use of logic synthesis has been made in the gate-array sections to reduce design time. This approach also permits rapid customization for future applications, whether they are in a more focused domain or to increase functionality. We believe that the combination of a highly optimized signal processing macroblock, together with the flexibility offered by synthesis in conjunction with gate-array (or standard cell), gives the architecture maximum potential for future applications. The prototype device has a target clock speed of 80 MHz (derived from Spice simulations of the PE's and memory, and HDL simulations of the major functional blocks taking account of layout and routing considerations), but the

TABLE I
COMPARISON OF DEVICES

Device	Clock Freq. (MHz)	Power Diss.	Tech.	Area (mmxmm)	Perf.*
VSP	80	6W"	0.7μm CMOS	13 x 13	1
ref [3]	300	13W	0.5μm BiCMOS	16.5 x 17	1
ref [4]	25	1W	0.8μm CMOS	15 x 15	0.125
ref [6]	50	1W	1μm CMOS	8.4 x 9.2	0.5

Performance is defined as the ability to perform H.261 coding on CIF images at 30 frames per second.
" Estimate.

architecture is specifically designed so that the array core is decoupled from the rest of the chip and we anticipate that future implementations will support array clock speeds of over 150 MHz. Rather than quote meaningless GOP figures (which can be massaged to any value depending upon how they are calculated) we prefer to quote realistic performance: When operating at the target clock speed (80 MHz), the chip will deliver the following *observable* performance (i.e., image input to fully computed results resident in external RAM). 16×16 MAC (14 b coefficient $\times$ 8 b data) at 750 K pixel.s^{-1}. 8×8 DCT (full 26 b intermediate precision) at 200 K DCT.s^{-1}. The array core is capable of fulfilling all the signal processing requirements of an H.261 codec with 30 Hz frame rate. Where operations can be internally pipelined on the array an equivalent performance of 2×10^6, 256 element 8×8 b signed multiply-accumulates per second can be delivered. The prototype has the following characteristics:

1) Technology: 0.7 μm TLM CMOS
2) RAMs: 4 K Data cache
3) 1.5 K Program cache
4) Pins: 169 (125 signal)
5) Core Array Size: 8×7 mm
6) Total Transistors: 1.7 M

Direct comparison of the architecture and design described in this paper with the devices outlined in Section I is difficult. However, Table I describes the salient features of these devices:

The differences in areas and performance of the other devices can be seen relative to the device which we describe. These other devices are all multipipeline architectures connected to internal memory blocks which are ported 4 ways (in many cases). These other architectures are specifically designed for image coding.

XI. CONCLUSION

We have presented an integrated approach to Video Signal Processing, featuring a new array based core signal processing architecture, which has specifically addressed the performance requirements of high speed 2-D functions found in image coding and computer vision applications. The design methodology adopted ensures that the device can quickly track any changes in available technology or application domain with a minimum of reengineering. The architecture has addressed two problems of conventional SIMD based machines: Providing high bandwidth, low latency IO coupled with an instruction set which minimizes instruction bandwidth and improves code density. The architectural features described have a wider application in any array Processor design.

ACKNOWLEDGMENT

The authors acknowledge the continuing support of J. Burnie and B. Holland.

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         (c) 1999 Business Wire
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Set     Items   Description
S1          0   SENSE(3N)AMPLIFIER?(5N)(SHARED OR USED)(3N)(ADJACENT? OR A-
             DJOIN?)(3N)ARRAY?
S2       4296    (INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN?)(3N)MEMORY(7N)CO-
             NTROLLER(3N)(IC OR INTEGRATED()CIRCUIT? OR CHIP?? OR CIRCUIT?-
             ?)
S3          0    (STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT
             OR PLACING)(3N)(ROW?? OR LINE?)(3N)(NONADJOIN? OR NONADJACENT?
              OR NON-ADJACEN?)(3N)ARRAY?
S4    3659502   VIDEO
S5       4338    (PLURAL? OR MANY OR SEVERAL OR NUMEROUS OR MANY OR MULTI OR
              MULTIPLE)(3N)(PIXEL? OR PEL OR PICTURE()ELEMENT? OR PICTURE(-
             3N)CELL??)
S6      18983   HORIZONTAL(3N)LINE?
S7      33431   IMAGE(3N)DISPLAY?
S8    2159055    (FIRST OR SECOND OR TWO OR 2 TOP OR BOTTOM)(3N)(HALF OR HA-
             LVES)
S9        100    (EVEN OR ODD)(3N)NUMBER?(3N)ARRAY?
S10     11969   FRAME(3N)BUFFER?
S11        41   PROCESSOR?(5N)(TRACK? OR MONITOR? OR DETECT? OR DETERMIN?)-
             (7N)(ACTIVE OR OPEN OR OFF)(5N)ARRAY??
S12         2   S4(S)S11
S13         1   RD S12 (unique items)
S14         0   S2(S)S4(S)S5(S)S6(S)S8(S)S9
S15         2   S2(S)S4(S)S5
S16         2   S15 NOT S12
S17         1   RD S16 (unique items)
S18       667   AU=(LAZAR P? OR YEO C? OR SELINGER D? OR KIM P? OR PINKHAM
             R? OR LAZAR, P? OR YEO, C? OR SELINGER, D? OR KIM, P? OR PINK-
             HAM, R?)
S19         0   AU=(PROEBSTING, R? OR PROEBSTING R?)
S20         0   S18 AND S10
S21         0   S18 AND SENSE(3N)AMPS
S22        44   S10(S)S5
S23         1   S22(S)S8
S24         0   S22(S)S9
S25         0   S22(S)S11
S26        11   S22 AND PY=1997:2004
S27        33   S22 NOT S26
S28        21   RD S27 (unique items)
S29         1    (NONADJACEN? OR NON-ADJACEN?)(3N)ARRAY??
```

13/3,K/1   (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06941022   Supplier Number: 58615530 (USE FORMAT 7 FOR FULLTEXT)
Getting Down With NT's Upside.(Marathon Technologies' Marathon Technologies Endurance 4000 network management software.)(Product Information)
Maley, Ryan
HP Professional, v13, n12, p51
Dec, 1999
Language: English   Record Type: Fulltext Abstract
Document Type: Magazine/Journal; Trade
Word Count: 917

...   demonstration at HP World, this highly redundant system seemed to work very well. Simply turning **off** various parts of the **array** simulated failures. For instance, turning **off** an I/O **Processor** yielded no net effect that I could **determine** with a streaming **video** playing on the system. Similarly, turning off a Compute Element caused no effect.
    Just as...

?

17/3,K/1 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

04018305 SUPPLIER NUMBER: 15386450
Multimedia powerhouse. (Texas Instruments MVP chip)
Guttag, Karl M.
Byte, v19, n6, p57(5)
June, 1994
ISSN: 0360-5280 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

ABSTRACT: Texas Instruments Inc's new Multimedia **Video** Processor (MVP) is a digital signal processing (DSP) tool that **integrates** five very powerful, fully programmable processors onto a single **chip** along with a sophisticated DMA **controller** with an external **memory** interface, 50KB of static RAM and **video** timing control. It involves three basic algorithmic areas: image processing and recognition, compression and fast...

...technology overcomes the problems traditional DSPs have had with processing bit-field manipulations and manipulating **multiple pixels** . The MVP's signal processors can manipulate bit fields and process **multiple pixels** in parallel. Most of the MVP's raw performance comes from its four ADSPs, each...
?

23/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01508559 SUPPLIER NUMBER: 12002302 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Finding the right video board. (new types of graphics boards mean users must choose carefully) (Hardware) (Tutorial)
Rowell, Dave
PC Sources, v3, n4, p119(3)
April, 1992
DOCUMENT TYPE: Tutorial ISSN: 1052-6579 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2596 LINE COUNT: 00196

... be generated by the CPU and moved into the memory chips that make up the **frame buffer** on the video card. Each time you scroll a screen at 1,024 by 768 resolution with a Super VGA board, for example, **two** and a **half** times as **many** **pixels** must be moved around by the CPU as with 640 by 480 resolution. That extra...
?

28/3,K/1 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(R)

1154378 Supplier Number: 01154378 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Opti chip set bucks using frame buffers
(Opti designs core-logic chip set for the Intel P6 CPU)
Electronic Engineering Times, n 841, p 1
March 27, 1995
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1268

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...s thinking may be based on a repartitioning of the graphics work load. Today, with **frame** **buffers**0 isolated from the CPU by a relatively slow bus such as PCI, it makes sense...

...back to the CPU. At more than 200 iSPECs, the P6 may be faster at **pixel** manipulation than **many** of the graphics controllers that would support it.

Such a partitioning also might reflect the...

28/3,K/2 (Item 2 from file: 9)
DIALOG(R)File 9:Business & Industry(R)

1102194 Supplier Number: 01102194 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Number Nine sets new OEM imaging strategy
(Number Nine Computer Corp to convert itself from a board maker into chip-to-board OEM provider of graphics and imaging subsystem elements)
Electronic Engineering Times, n 830, p 99
January 09, 1995
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1057

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...user that's what's important."

Big price

For example, the Imagine processor creates virtual **pixel** maps and mixes **multiple** video streams in the **frame** **buffer** , he said. "Our approach to graphics is more like what Silicon Graphics is doing," Najda...

28/3,K/3 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00652433 93-01654
High-Performance Graphics Made Simple
Martin, Robert; Martin, Claudia

CAE v11n11 PP: 42-48 Nov 1992
ISSN: 0733-3536 JRNL CODE: CAE
WORD COUNT: 2446

...ABSTRACT: of points called pixels (picture elements) that are addressable by computer memory. Resolution describes how **many pixels** fit on the screen and is calculated as the number of horizontal pixels by the...

... the monitor is capable. Video controllers, or graphics boards, can be divided into 3 categories: **frame buffers** , fixed-function graphic accelerators, and true programmable graphics coprocessors. True graphics coprocessors are fully programmable...

28/3,K/4 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03746464 Supplier Number: 45318154 (USE FORMAT 7 FOR FULLTEXT)
IBM DAC INSERTS YUV-RGB CONVERSION
Electronic News (1991), p56
Feb 6, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 698

... solutions required separate channels while IBM's RGB624, by being fully programmable and offering simultaneous **multiple pixel** formats, enables designs to use only one **frame buffer** , Mr. West said.
As a result, the same physical memory bits are used to store...

28/3,K/5 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

03694382 SUPPLIER NUMBER: 11657502 (USE FORMAT 7 OR 9 FOR FULL TEXT)
24-bit graphics adapters: true color and plenty of horsepower. (Hardware Review) (overview of six evaluations of 24-bit graphics adapters)(includes glossary, editors' choice and related articles on testing methodologies) (Evaluation)
Karney, James; Quain, John R.; Ehrenman, Gayle C.
PC Magazine, v11, n1, p263(20)
Jan 14, 1992
DOCUMENT TYPE: Evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4875 LINE COUNT: 00367

... block transfer)
An operation in which the pixel data residing in one area of the **frame buffer** is copied to another area of the **frame buffer** or to system memory, and vice versa. By performing bit-block transfers, graphics coprocessors can...

...video display speeds, since a displayed object is treated as one unit rather than as **many** individual **pixels** .
DAC (digital-to-analog converter)
A chip that converts the binary numbers that represent particular...

28/3,K/6 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08010122 SUPPLIER NUMBER: 16864044 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Optic chip set bucks using frame buffers. (Opti Inc Mustang chip set marks end of PC AT architecture)
Wilson, Ron
Electronic Engineering Times, n841, p1(2)
March 27, 1995
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1372 LINE COUNT: 00108

... back to the CPU. At more than 200 iSPECs, the P6 may be faster at **pixel** manipulation than **many** of the graphics controllers that would support it.
Such a partitioning also might reflect the...

28/3,K/7 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07719249 SUPPLIER NUMBER: 16644519 (USE FORMAT 7 OR 9 FOR FULL TEXT)
IBM DAC inserts YUV-RGB conversion.(IBM MIcroelectronics introduces RGB624 digital-to-analog converter)(Product Announcement)
Krause, Reinhardt
Electronic News (1991), v41, n2051, p56(1)
Feb 6, 1995
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 753 LINE COUNT: 00058

... being fully programmable and offering simultaneous multiple pixel formats, enables designs to use only one **frame buffer** , Mr. West said.
As a result, the same physical memory bits are used to store...

28/3,K/8 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

04042550 SUPPLIER NUMBER: 07478934
A planar picture. (planar architecture)
Wynia, Todd
Electronic Engineering Times, n549, p23(2)
July 31, 1989
ISSN: 0192-1541 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

...ABSTRACT: in parallel is an inexpensive way to increase performance and pixel depth. The data for **multiple pixels** is stored in separate memory chips in a planar architecture, making it easy to access **multiple pixels** and process them in parallel. Thus, with the addition of a separate processor to access...

28/3,K/9 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03321468   SUPPLIER NUMBER: 05132173   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Video palette raises color ante to 1024 separate hues.
Mokhoff, Nicolas
Electronic Design, v35, p43(3)
Aug 20, 1987
ISSN: 0013-4872   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 1645   LINE COUNT: 00124

...   1) enable TTL-compatible interfacing with incoming data lines up to 45 MHz to the **frame buffer**, while maintaining the 135-MHz video data rate. The programable multiplexers allow designers to build a **frame buffer** with the fewest possible memory chips.
After considering user needs, designers came up with Bt461...

28/3,K/10   (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03289519   SUPPLIER NUMBER: 05074170   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pipelined graphics engine speeds 3-D image control.
Burgoon, Dave
Electronic Design, v35, p143(6)
July 23, 1987
ISSN: 0013-4872   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 3714   LINE COUNT: 00289

...   a compare. Accepted pixels need a Z read, a Z write, a compare, and a **frame - buffer** write of the color. If these functions must be done from 1 to 5 million...

28/3,K/11   (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03289511   SUPPLIER NUMBER: 05074162   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Custom VLSI chips soup up graphics engines.
Mokhoff, Nicolas
Electronic Design, v35, p33(3)
July 23, 1987
ISSN: 0013-4872   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 1542   LINE COUNT: 00123

...   Fairchild Semiconductor is developing a set of chips that will allow frame buffers to access **multiple pixels** in one memory cycle, with optimal orientation for each operation regardless of the ultimate screen positioning. This sidesteps the classical bandwidth limits of current commercial **frame buffers**, because they can access only one pixel per memory cycle when speed is critical in...

28/3,K/12   (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03119580   SUPPLIER NUMBER: 04683059   (USE FORMAT 7 OR 9 FOR FULL TEXT)
200-MHz FIFO buffer juggles multiple windows.
Pieper, Steve; Garbe, Olivier

Electronic Design, v35, p95(3)
Feb 5, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2078 LINE COUNT: 00151

... to access the window data.

Because a display memory word is several pixels wide, the **frame - buffer** controller normally places window boundaries only at display memory-word boundaries rather than at pixel...end-bit address of the window boundary on the ACD bus along with the last **pixel** word.

Several factors determine the maximum number of hardware windows that the system can simultaneously scroll and...

...first consideration is the rate at which the FIFO buffer can be filled when the **frame buffer** is supplying data to it at one end while video data is flowing from the...

28/3,K/13 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01859563
National Semi sampling Raster Graphics processor
Electronic News January 25, 1988 p. 32
ISSN: 0013-4937

...384 x 16,384 pixels/bitmap and supports text character size to 256 x 256 **pixels** along with **multiple** font sizes and proportional spacing. It features a general-purpose microcoded microprocessor, a programmable video ...

...Bitblt controller and a rectangular clipper. It operates with all memory types and can access **frame buffers** in planar or pixel fashion with the 2 modes selectable on an operation-by-operation...

28/3,K/14 (Item 2 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01025029
New product previews: High-speed graphics chip set reduces burden on host microprocessor.
Electronics May 3, 1984 p. 84,186

... speed drawing line times are due to an architecture that allows GMP to fill in **multiple pixels** during a single memory cycle. The firm's associated Video Shift Register (VSR) circuit, to...

... a CMOS gate array to support the GMP. VSR chip functions include data bus control, **frame buffer** , and the conversion of parallel pixel data from the **frame buffer** into the serial form needed to drive a color-pallet random access memory. To be...

28/3,K/15 (Item 3 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

00974649
Powerful new microcomputers make possible high-quality graphics systems, connecting visual devices that formerly were not even considered computer peripherals, eg, VTRs, special Polaroid cameras, and typesetting machines.
Infoworld December 19, 1983 p. 34-361

... symbols that explain and illuminate subtle or complex relationships with Lisa's b&w, 720x364 **pixels** , professional-quality screen. **Many** IBM-compatible packages also are becoming available. For example, PC Plus (Frederick, Maryland) offers the...

... California) sells a variety of computer-graphics systems based on the graphics memory card--the **frame buffer** . The firm sells a hardware and software kit that turns the IBM PC into a graphics computer, including software, color monitor, a **frame buffer** and a digitizing tablet.
...

28/3,K/16 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01749760 SUPPLIER NUMBER: 16641843 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Basic windows.(Graphics Cards Up the Ante)
Plain, Stephen W.
Windows Sources, v00000003, n4, p124(7)
April, 1995
ISSN: 1065-9641 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3586 LINE COUNT: 00273

... video memory it provides and how it utilizes this memory. With most accelerators, a 2MB **frame buffer** will let you use 24-bit true color at resolutions as high as 800 by...the pixel information. The unaligned memory writes also put a heavier burden on the CPU. **Many** boards that use **pixel** packing also provide unpacked, 24-bit true-color modes for those who want better performance...

28/3,K/17 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01749750 SUPPLIER NUMBER: 16641823 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Less is more.(The Critical Distinctions)(Getting Win 95 Up to Speed)(Column)(Tutorial)
Smith, Gregory
Windows Sources, v00000003, n4, p77(1)
April, 1995
DOCUMENT TYPE: Column Tutorial ISSN: 1065-9641 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 449 LINE COUNT: 00034

... DIB) engine. The DIB engine assumes that your graphics board allows direct access to the **frame buffer** and that your display device uses a packed-pixel format. The packed-pixel format, where...

...sequence, is quite common. Still, if your graphics card uses a planar format (where each **pixel** appears in **several** planes--one for each color) your vendor will have to write the entire graphics driver...

28/3,K/18 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01508559 SUPPLIER NUMBER: 12002302 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Finding the right video board. (new types of graphics boards mean users must choose carefully) (Hardware) (Tutorial)
Rowell, Dave
PC Sources, v3, n4, p119(3)
April, 1992
DOCUMENT TYPE: Tutorial ISSN: 1052-6579 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2596 LINE COUNT: 00196

... be generated by the CPU and moved into the memory chips that make up the **frame buffer** on the video card. Each time you scroll a screen at 1,024 by 768 resolution with a Super VGA board, for example, two and a half times as **many pixels** must be moved around by the CPU as with 640 by 480 resolution. That extra...

28/3,K/19 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03065141 Supplier Number: 46266074 (USE FORMAT 7 FOR FULLTEXT)
SPECIAL REPORT: VideoLogic, Inc.
PCNetter, v11, n4, pN/A
April 1, 1996
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 3753

... are fetched and are used to texture each pixel before it is written into the **frame buffer** . Depending on the exact texturing technique, different numbers of texels are needed per output pixel...

...associated polygon. Point-sampling techniques can result in the same texel value being used for **several** adjacent output **pixels** , depending on the orientation of the polygon--and this can result in "blockiness" of the ...

28/3,K/20 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01047944 CMP ACCESSION NUMBER: EET19950327S0005
Opti chip set bucks using frame buffers
Ron Wilson
ELECTRONIC ENGINEERING TIMES, 1995, n 841, PG1
PUBLICATION DATE: 950327
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 1259

... s thinking may be based on a repartitioning of the graphics work

load. Today, with **frame buffers** isolated from the CPU by a relatively slow bus such as PCI, it makes sense...

...back to the CPU. At more than 200 iSPECs, the P6 may be faster at **pixel** manipulation than **many** of the graphics controllers that would support it.

Such a partitioning also might reflect the...

28/3,K/21 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00635549 CMP ACCESSION NUMBER: EET19890731S3673
A planar picture
TODD WYNIA (PRODUCT MARKETING MANAGER HEURIKON CORP. MADISON, WIS.)
ELECTRONIC ENGINEERING TIMES, 1989, n 549, 23
PUBLICATION DATE: 890731
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: TECHNOLOGY
WORD COUNT: 1145

... conventional packed pixel architecture, the data associated with each pixel is stored contiguously in the **frame buffer** . Because a single RAM may contain data for **multiple pixels** , it is difficult to design a parallel access scheme in which **multiple pixels** may be accessed and processed simultaneously. For that reason, packed pixel systems must typically use a single processor to access the entire **frame buffer** , causing throughput to decrease as an inverse function of pixel depth.

Because their performance varies...

?

29/3,K/1 (Item 1 from file: 88)
DIALOG(R)File 88:Gale Group Business A.R.T.S.

04898633 SUPPLIER NUMBER: 21109811
On association, realization, and form in Richard Swift's 'Things of August.' (1985 musical piece by composer)
Hanninen, Dora A.
Perspectives of New Music, v35, n1, p61(54)
Wntr, 1997
ISSN: 0031-6016 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 15777 LINE COUNT: 01257

... repetitions, others three; a given pc may be repeated in two or three adjacent or **nonadjacent array** columns.

Vertical pc weighting differs from horizontal pc weighting in a crucial respect: for each...
?

```
File   2:INSPEC 1969-2004/Mar W3
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Mar W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Mar W3
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Mar W3
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Mar W4
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Mar W2
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File 144:Pascal 1973-2004/Mar W3
         (c) 2004 INIST/CNRS
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2004/Mar 27
         (c) 2004 ProQuest Info&Learning
File 248:PIRA 1975-2004/Mar W2
         (c) 2004 Pira International

Set     Items   Description
S1          1   SENSE(3N)AMPLIFIER? AND (SHARED OR USED)(3N)(ADJACENT? OR -
             ADJOIN?)(3N)ARRAY?
S2        102   (INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN?)(3N)MEMORY AND C-
             ONTROLLER(3N)(IC OR INTEGRATED()CIRCUIT? OR CHIP?? OR CIRCUIT-
             ??)
S3          0   (STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT
             OR PLACING)(3N)(ROW?? OR LINE?)(3N)(NONADJOIN? OR NONADJACENT?
              OR NON-ADJACEN?)(3N)ARRAY?
S4     422739   VIDEO
S5       2757   (PLURAL? OR MANY OR SEVERAL OR NUMEROUS OR MANY OR MULTI OR
              MULTIPLE)(3N)(PIXEL? OR PEL OR PICTURE()ELEMENT? OR PICTURE(-
             3N)CELL??)
S6       8254   HORIZONTAL(3N)LINE?
S7      18582   IMAGE(3N)DISPLAY?
S8     157869   (FIRST OR SECOND OR TWO OR 2 TOP OR BOTTOM)(3N)(HALF OR HA-
             LVES)
S9        125   (EVEN OR ODD)(3N)NUMBER?(3N)ARRAY?
S10      1862   FRAME(3N)BUFFER?
S11       579   PROCESSOR? AND (TRACK? OR MONITOR? OR DETECT? OR DETERMIN?)
              AND (ACTIVE OR OPEN OR OFF) AND ARRAY??
S12        12   AU=(PROEBSTING, R? OR PROEBSTING R?)
S13         0   S2 AND S9
S14       237   S4 AND S5
S15         0   S14 AND S9
S16         0   S14 AND S11
S17         0   S14 AND S2
S18         0   S14 AND S6 AND S7 AND S8
```

S19	7	S14 AND S6:S8
S20	7	S19 NOT S1
S21	1	S20 AND PY=1997:2004
S22	6	S20 NOT S21
S23	6	RD S22 (unique items)
S24	0	S12 AND S2
S25	0	S12 AND S5
S26	0	S12 AND S4
S27	18	S2 AND S4
S28	4	S27 AND (BANK?? OR ARRAY?)
S29	4	S28 NOT (S1 OR S19)
S30	2	S29 AND PY=1997:2004
S31	2	S29 NOT S30
S32	2	RD S31 (unique items)
S33	14	S27 NOT (S1 OR S19 OR S28)
S34	2	S33 AND PY=1997:2004
S35	12	S33 NOT S34
S36	9	RD S35 (unique items)
S37	0	S5 AND S9
S38	22	S5 AND S10
S39	3	S38 AND PY=1997:2004
S40	19	S38 NOT S39
S41	19	S40 NOT (S27 OR S1 OR S19 OR S28)
S42	0	S41 AND PY=1997:2004
S43	11	RD S41 (unique items)
S44	1	(STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT OR PLACING) AND (ROW?? OR LINE?) AND (NONADJOIN? OR NONADJACENT? OR NON-ADJACEN?) AND ARRAY?

1/3,K/1   (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01870372 ORDER NO: AADAA-IMQ63029
Design and implementation of a 16kbit 1T1C ferroelectic random access memory testchip
Author: Siu, Joseph Wai-Kit
Degree: M.A.Sc.
Year: 2001
Corporate Source/Institution: University of Toronto (Canada) (0779)
Source: VOLUME 40/03 of MASTERS ABSTRACTS.
PAGE 760. 62 PAGES
ISBN: 0-612-63029-3

...thesis presents design and implementation of a novel reference generation scheme and a current-steering **sense** amplifier . The reference generation scheme balances fatigue among memory cell capacitors and reference cell capacitors on the same row. The **sense** **amplifier** design allows a reference current to be **shared** among eight **adjacent** columns in the memory **array** .

A 16kbit 1T1C ferroelectric random access memory (FeRAM) testchip has been designed and fabricated in...
?

23/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5161432 INSPEC Abstract Number: B9602-6140C-313, C9602-5260B-216
Title: A RISC controlled motion estimation processor for MPEG-2 and HDTV encoding
Author(s): Charlot, D.; Bard, J.-M.; Canfield, B.; Cuney, C.; Graf, A.; Pirson, A.; Teichner, D.; Yassa, F.
Author Affiliation: Thomson Consumer Electron. Components, Meylan, France
Conference Title: 1995 International Conference on Acoustics, Speech, and Signal Processing. Conference Proceedings (Cat. No.95CH35732) Part vol.5 p.3287-90 vol.5
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 5 vol. 3662 pp.
ISBN: 0 7803 2431 5 Material Identity Number: XX95-01000
U.S. Copyright Clearance Center Code: 0 7803 2431 5/94/$4.00
Conference Title: 1995 International Conference on Acoustics, Speech, and Signal Processing
Conference Sponsor: Signal Process. Soc. IEEE
Conference Date: 9-12 May 1995 Conference Location: Detroit, MI, USA
Language: English
Subfile: B C

...Abstract: can also be used in HDTV applications. The motion estimation processing is in 2 steps: **first** full- **pixel** then **half - pixel** . **Several** modes are possible, depending on the image types (I, P or B-MPEG terminology, frame...
...Descriptors: **video** coding

23/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03513769 INSPEC Abstract Number: C90002038
Title: A modular approach to image processing through the VMEbus
Author(s): de Sa, L.; Dias, J.; Silva, V.
Author Affiliation: Dept. de Engenharia Electrotecnica, Coimbra Univ., Portugal
Conference Title: VMEbus in Research. Proceedings of an International Conference p.83-9
Editor(s): Eck, C.; Parkman, C.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1988 Country of Publication: Netherlands xx+494 pp.
ISBN: 0 444 70524 4
Conference Sponsor: Eur. Stand. Nucl. Electron
Conference Date: 11-13 Oct. 1988 Conference Location: Zurich, Switzerland
Language: English
Subfile: C

...Abstract: of a VMEbus based computer. In a typical configuration the system uses one module for **image** acquisition and **display** and **several** modules for **pixel** processing. Each pixel processing module, based on a DSP processor, operates on a fraction of...
... to all pixel processing boards present in the system by a private 130 Mbits/s **video** bus built around the P2 connector.
...Identifiers: private 130 Mbits/s **video** bus...

23/3,K/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01800743 E.I. Monthly No: EI8509076751 E.I. Yearly No: EI85031680
Title: VIDEO **MODE PLASMA PANEL USING LIGHT PEN.**
Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 2 Jul 1985 p 585
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH

Title: VIDEO **MODE PLASMA PANEL USING LIGHT PEN.**
...Abstract: the information presented on a plasma display panel, the plasma panel can operate in a **video** refresh mode. All the data on a **horizontal line** are written simultaneously in one cycle rather than serially in a horizontal scan, such as a cathode ray tube display. This means that the **many** pels (**picture elements**) on the line cannot be time discriminated; however, with the panel content in storage, test...
Identifiers: PLASMA PANEL; PLASMA DISPLAY; **VIDEO** REFRESH MODE; LIGHT-PEN DETECTION

23/3,K/4 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00782240 F94076035942
Fast display for real-time electrical impedance tomography
(Ein schnelles Display fuer die elektrische Impedanztomographie in Echtzeit)
Sinton, AM; Smith, RWM; McArdle, FJ; Brown, BH
Dep. of Med. Physics a. Cinical Engng., Univ. of Sheffield, Royal Hallamshire Hosp., Sheffield, GB
Proc. of the 14th Annual Int. Conf. of the IEEE Engineering in Med. and Biol. Soc., Part. 5, Paris, F, Oct 29 - Nov 1, 19921992
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-7803-0785-2; 0-7803-0786-0

ABSTRACT:
This paper describes the fast **image display** of the Sheffield Real-Time Electrical Impedance Tomograph. The display uses standard Transputer-based graphics hardware driving a CRT **video** monitor. It produces a large, interpolated, movie display on the CRT screen at 25 images...

...second, and is capable of operating several times faster than this. To be useful, the **displayed image** must appear large enough on the CRT screen to be viewable from a reasonable distance...

...arranged in a circle inscribed within a square of 16 x 16 pixels. If this **image** were **displayed** directly on a typical **image display** of, say, 512 x 512 **display** pixels, with each **image** pixel occupying one **display** pixel, the **displayed image** would be too small, e.g. only 7 mm diameter on a typical 14-inch diagonal CRT monitor. To produce a big **displayed image** each **image** pixel must be spread out over **many** display **pixels** . This effectively is a two-dimensional interpolation in the **display** between **image** pixels. The challenge is to perform this interpolation and display the result quickly, without requiring...

...DESCRIPTORS: APPLIED POTENTIAL TOMOGRAPHY; FRAME SPEED; **VIDEO** TECHNIQUE; CATHODE RAY TUBE; DATA DISPLAY; DATA OUTPUT; REAL TIME METHOD; GRAPHIC DATA PROCESSING; IMAGE...

23/3,K/5 (Item 1 from file: 248)
DIALOG(R)File 248:PIRA

00077834 Pira Acc. Num.: 40710721
Title: SYSTEM FOR CONVERTING NUMBER OF SCANNING LINES
Authors: Kasuga Masa; Takahashi Nobuaki; Shibamoto Takeshi
Patent Assignee: VICTOR COMPANY OF JAPAN LIMITED
Patent Number: US 4471381 Application Date: 840911
Document Type: Patent
Language: unspecified

...Abstract: number of scanning lines converts a first number of scanning lines of a first digital **video** signal into a second number of scanning lines of a second digital **video** signal. The system comprises a discrete signal obtaining circuit supplied with the first digital **video** signal, for successively re-arranging a **plurality** of **picture** **element** information arranged along lines in a vertical direction with respect to a picture frame indicated by the first digital **video** signal within a time interval corresponding to the first number of scanning lines in units...

... signal having a sampling frequency equal to a horizontal scanning frequency of the first digital **video** signal, a sampling frequency converter for converting the sampling frequency of the discrete signal obtained...
... obtaining circuit into a frequency equal to a horizontal scanning frequency of the second digital **video** signal, and a second **video** signal obtaining circuit for successively re-arranging an output of the sampling frequency converter in units of a **plurality** of **picture** **element** information along a direction of **horizontal** scanning **lines** in accordance with the second digital **video** signal in a time series manner, to obtain the second digital **video** signal using the second number of scanning lines.

23/3,K/6 (Item 2 from file: 248)
DIALOG(R)File 248:PIRA

00076935 Pira Acc. Num.: 40607058
Title: NOISE REDUCTION IN DIGITAL FLUOROSCOPY SYSTEMS
Authors: Riederer Stephen
Patent Assignee: GENERAL ELECTRIC COMPANY
Patent Number: US 4367490
Application Date: 830104
Document Type: Patent
Language: unspecified

...Abstract: the effect of x-ray statistical noise and electronic noise in a fluorographic system that **displays** an x-ray **image** on a television screen. Analog **video** signals based on the x-ray image are amplified logarithmically and digitized to yield live...

... a noise reduction multiplicative factor, K. The other part of the addresses is the live **pixel** value. There are **several** replications of

32/3,K/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00779800 JICST ACCESSION NUMBER: 89A0571308 FILE SEGMENT: JICST-E
Development of color still- video **telephone.**
ISHIKAWA YASUNORI (1); SATO KEI (1); KUWATA KOJI (1); SHIMURA HIROSHI (1); ISHIKAWA MASAAKI (1)
(1) Ricoh Co., Ltd., Res. and Development Center
Ricoh Tech Rep, 1989, NO.19, PAGE.34-40, FIG.10, TBL.8, REF.6
JOURNAL NUMBER: Z0825AAU ISSN NO: 0387-7795
UNIVERSAL DECIMAL CLASSIFICATION: 621.395
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

Development of color still- video **telephone.**
ABSTRACT: This paper describes a recently developed Color Still- **Video** Telephone which uses an analog telephone network. In general, image transmission requires a wide-band...

...compression and communication protocol technology using G3 FAX MODEM has been developed. In addition, by **integrating** high-performance **memory** /display **controller** **circuitry**0 into a Gate- **Array** and applying color CCD **video** camera and color LCD, all functional parts can be enclosed into one small unit, which...
...DESCRIPTORS: **video** telephone

32/3,K/2 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00336359 94BY01-008
Intel/VLSI join the PDA fray -- A new PDA chip set from Intel and VLSI brings the 80x86 architecture to PDAs
Statt, Paul
BYTE , January 1, 1994 , v19 n1 p101-105, 5 Page(s)
ISSN: 0360-5280
Company Name: Intel Corp.; VLSI; Advanced Micro Devices; AT&T
Product Name: Polar; Am386SC; Hobbit

... Integrated Processor Controller (IPC), a 32-bit processor architecture based on the Intel 386, which **integrates** **memory** management, **video** control, and power management. Notes that the IPC includes a cache controller with an integrated...

... tag RAM, and it handles both volatile and nonvolatile memory (NVM). Claims that the large **array** , NVM interface is tuned for high-performance XIP code, as well as for data storage, and the page-mode DRAM **controller** supports different **chip** configurations. Explains that the IPC integrates a 640-by-480-pixel LCD controller and an...
?

36/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4673731 INSPEC Abstract Number: C9407-5540-001
Title: A low-cost graphics and multimedia workstation chip set
Author(s): Undy, S.; Bass, M.; Hollenbeck, D.; Kever, W.; Thayer, L.
Author Affiliation: Hewlett-Packard Co., Fort Collins, CO, USA
Journal: IEEE Micro vol.14, no.2 p.10-22
Publication Date: April 1994 Country of Publication: USA
CODEN: IEMIDZ ISSN: 0272-1732
U.S. Copyright Clearance Center Code: 0272-1732/94/$04.00
Language: English
Subfile: C

...Abstract: floating-point unit, a 1-Kbyte internal instruction cache, an integrated external cache controller, an **integrated memory** and I/O controller, plus enhancements for little-endian and multimedia applications. Its Artist graphics controller integrates a graphical user interface accelerator, a frame buffer controller, and a **video controller** on a single **chip** .
...Identifiers: **video** controller

36/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03350886 INSPEC Abstract Number: B89022788, C89026325
Title: An image memory controller chip
Author(s): Stoner, D.T.; Norsworthy, J.P.; Corry, M.K.
Author Affiliation: Visual Information Technologies Inc., Plano, TX, USA
Conference Title: Electronic Imaging '88: International Electronic Imaging Exposition and Conference. Advance Printing of Paper Summaries p.668-70 vol.2
Publisher: Inst. Graphic Commun, Waltham, MA, USA
Publication Date: 1988 Country of Publication: USA 2 vol. xxxviii+1272 pp.
Conference Sponsor: Diagnostic Imaging Magazine; ESD:Electron. Syst. Design Magazine; et al
Conference Date: 3-6 Oct. 1988 Conference Location: Boston, MA, USA
Language: English
Subfile: B C

Title: An image memory controller chip
Abstract: The VITec image memory **controller** (IMC) **chip** is an experimental chip representing a condensation of all of the system, image memory, and **video** control functions within the VITec Image Computing System. Its development was driven out of the...
... the requirements of the system. The main functions of the chip are: system clock generation; **memory** control (**including** the formatting of linear addresses to DRAM compatible ones, DRAM refresh, and **video** DRAM shift register loads); memory request arbitration; and **video** control generation. The IMC serves as the indefatigable 'man-behind-the-scenes', enabling harmonious operation of the image memory, image processor, host processor, and **video** system modules within an image computing system.
...Descriptors: **video** signals
Identifiers: VITec image memory **controller chip** ; ...

... **video** control functions...

... **video** DRAM shift register loads...

... **video** system modules

36/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03310419 INSPEC Abstract Number: B89014874, C89012425
Title: A VLSI controller for flicker free television display
Author(s): Orben, H.-J.
Author Affiliation: ITT Semicond., Frieburg, West Germany
Journal: IEEE Transactions on Consumer Electronics vol.34, no.3 p. 420-5
Publication Date: Aug. 1988 Country of Publication: USA
CODEN: ITCEDA ISSN: 0098-3063
U.S. Copyright Clearance Center Code: CH2564-3/88/0800-0420$01.00
Conference Title: 1988 International Conference on Consumer Electronics (ICCE '88)
Conference Sponsor: IEEE
Conference Date: 8-10 June 1988 Conference Location: Rosemount, IL, USA
Language: English
Subfile: B C

...Abstract: VLSI) chip is presented that provides a 100-Hz flicker-free television display. Only one **controller chip** with six standard dynamic random-access memories (DRAMs) are used. The **video** memory **controller chip** , fabricated in a 1.5- mu m CMOS process, works with all the common television...
...Descriptors: **integrated memory** circuits
...Identifiers: **controller chip** ; ...

... **video** memory **controller chip** ;

36/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

01544749 INSPEC Abstract Number: B80036946
Title: Simplify CRT-system design with transparent addressing-it comes on a controller chip
Author(s): Boisvert, C.
Author Affiliation: Synertek Inc., Santa Clara, CA, USA
Journal: Electronic Design vol.27, no.16 p.90-3
Publication Date: 2 Aug. 1979 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
Language: English
Subfile: B

Title: Simplify CRT-system design with transparent addressing-it comes on a controller chip
Abstract: Discusses microprocessor based CRT systems and describes how to incorporate transparent addressing with a CRT **controller chip** that **includes memory** addressing right on the chip and makes the system CPU transparent to the system's...
...Identifiers: CRT **controller chip** ; ...

... **video** interface

36/3,K/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02086901 E.I. Monthly No: EIM8604-024966
Title: SEMICONDUCTOR TRENDS IN COMPUTER GRAPHICS.
Author: Wientjes, Brent R.
Corporate Source: Texas Instruments Inc, Houston, TX, USA
Conference Title: Proceedings - CADCON Central, Computer-Aided Design Engineering Conference.
Conference Location: Dallas, TX, USA Conference Date: 19841030
E.I. Conference No.: 07286
Source: Publ by Morgan-Grampian Publ Co, New York, NY, USA p V. 12-V. 13
Publication Year: 1984
Language: English

...Abstract: graphics present major economic opportunities to allow semiconductor companies to develop dedicated graphic components. Illustrations **include** the TMS4161 Multiport **Memory** and **Video** System **Controller** **circuits** . Additional performance enhancements are in order in the near future.

36/3,K/6 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00884697 I95044920258
Pixel processing in a memory controller
(Die Implementierung eines programmierbaren Pixel-Prozessor in einem Speicher- **Controller** - **Chip** einer Workstation)
Donovan, W; Sabella, P; Kabir, I; Hsieh, MM
IEEE Computer Graphics and Applications, v15, n1, pp51-61, 1995
Document type: journal article Language: English
Record type: Abstract
ISSN: 0272-1716

(Die Implementierung eines programmierbaren Pixel-Prozessor in einem Speicher- **Controller** - **Chip** einer Workstation)

ABSTRACT:
The SX-a programmable pixel processor implemented in a workstation memory **controller** **chip** -aims to perform as well as low-end 2D and 3D graphics processors and to...

...large internal register set; vectorized RISC-like instruction set; fast access to both main and **video** memory; fast pixel operations; free operations; unpolluted cache; and single-chip solution. We describe the...
...DESCRIPTORS: SEMICONDUCTORS; IMAGE PROCESSING; GRAPHIC DATA PROCESSING; IMPLEMENTATION; WORK STATIONS; MICROCONTROLLERS; **INTEGRATED** **MEMORY** CIRCUITS; GRAPHICS PROCESSORS; REGISTER...
IDENTIFIERS: COMPUTER GRAPHIC EQUIPMENT; TESTS; IMAGE PROCESSING EQUIPMENT; WORKSTATION MEMORY **CONTROLLER** **CHIP** ; SX PROGRAMMABLE PIXEL PROCESSOR; LARGE INTERNAL REGISTER SET; VECTORIZED RISC LIKE INSTRUCTION SET; FAST ACCESS; **VIDEO** MEMORY; FAST PIXEL OPERATIONS; FREE OPERATIONS; UNPOLLUTED CACHE; SINGLE CHIP SOLUTION; WORKSTATION CONFIGURATION; SX PROCESSOR

ARCHITECTURE; SAMPLE ALGORITHMS; SX PERFORMANCE; PROGRAMMIERBARER PIXEL PROZESSOR; programmierbarer Pixel-Prozessor; Speicher- **Controller** - **Chip**

36/3,K/7 (Item 2 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00620490 I92038560938
ASIC design in a next generation workstation
(Der Entwurf von Kundenschaltungen fuer Workstations der naechsten Generation)
Young, MS
Sun Microsystems Inc., Mountain View, CA, USA
Proceedings. Third Annual IEEE ASIC Seminar and Exhibit, 17-21 Sept. 1990, Rochester, NY, USA1990
Document type: Conference paper Language: English
Record type: Abstract

ABSTRACT:
...machine to the Sparcstation 1 are discussed. The design team partitioned the design into four **chips** : the cache **controller** (CACHE+), memory management unit (MMU+), direct memory access (DMA+), and dynamic memory controller (RAM+). Architectural...

...of one of the ASICs from two to one part per board. One ASIC, a **video** controller, was reused. The manpower requirements of the project and the design/verification tools used...
...IDENTIFIERS: NEXT GENERATION WORKSTATION; FOLLOW ON MACHINE; CACHE CONTROLLER; MEMORY MANAGEMENT UNIT; DIRECT MEMORY ACCESS; DYNAMIC **MEMORY** CONTROLLER; HIGHER **INTEGRATION** ; **VIDEO** CONTROLLER; CAD; Mikrocontroller; Pufferspeicher

36/3,K/8 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00300659 93PI01-167
Flash 486DX2-66E
Rist, Oliver
PC Magazine , January 26, 1993 , v12 n2 p208, 1 Page(s)
ISSN: 0888-8507
Company Name: National Microsystems
Product Name: Flash 486DX2-66E

... the integrated touches offered by other systems such as integrated I/O ports and drive **controller** **circuits** , flash-upgradable BIOS, and an upgradable CPU path. Benchmark tests resulted in high scores for...

... under DOS, a characteristic of systems using the S3 graphics accelerator, even with local bus **video** . Processor scores were average, **memory** scores slightly below. **Includes** one photo, one illustration. (djd)

36/3,K/9 (Item 1 from file: 583)
DIALOG(R)File 583:Gale Group Globalbase(TM)

03430514
ROHM DEVELOPS TITLE MEMORY CONTROL IC
JAPAN - ROHM DEVELOPS TITLE MEMORY CONTROL IC
Journal of the Electronics Industry (JEI) 0 April 1990 p71
ISSN: 0385-4515

Rohm has developed the BU2728K, a camera- **integrated** VCR title **memory controller IC** , the BA6458FP, a VCR cylinder 3-phase motor driver IC, and the BA6440FP, a VCR...

PRODUCT: **Video** Equipment
?

43/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5264093 INSPEC Abstract Number: B9606-6140C-457, C9606-5260B-321
Title: Pilot model of the "extra high quality imaging system"
Author(s): Taniho, S.; Ito, H.; Moriwaki, H.; Katada, H.; Makino, S.
Author Affiliation: Dept. of Comput. Display Syst. Dev., Nanao Corp., Ishiwaka, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2663 p.36-9
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1996 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2663L.36:PMTH;1-8
Material Identity Number: C574-96076
U.S. Copyright Clearance Center Code: 0 8194 2037 9/96/$6.00
Conference Title: Very High Resolution and Quality Imaging
Conference Sponsor: SPIE; Soc. Imaging Sci. & Technol
Conference Date: 31 Jan.-2 Feb. 1996 Conference Location: San Jose, CA, USA
Language: English
Subfile: B C
Copyright 1996, IEE
...Abstract: B, 12 bits respectively.) This system comprises a MO disk drive, a controlling computer, a **frame buffer** and two 21" displays. The 2048*2048 pixel (36 bits/pixel) image data are read from the MO disk drive, and are sent to the **frame buffer** . A deliberately constructed 16 M byte **frame buffer** outputs the 36 bits/pixel video signal at a 200 MHz clock rate. Two displays...

... to compare the image quality of 36 bits/pixel system with that of 24 bits/ **pixel** system. **Many** characteristics and physical factors including noise, which do not cause a serious problem in conventional...
...Identifiers: **frame buffer ;**

43/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4437323 INSPEC Abstract Number: B9308-6140C-105, C9308-5530-004
Title: A Matlab/TMS320/TMS340 image processing environment
Author(s): Marshall, T.G., Jr.
Author Affiliation: Dept. of Electr. Eng., Rutgers Univ., Piscataway, NJ, USA
Conference Title: 1992 IEEE International Symposium on Circuits and Systems (Cat. No.92CH3139-3) p.2505-8 vol.5
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA 6 vol. 3028 pp.
ISBN: 0 7803 0593 0
U.S. Copyright Clearance Center Code: 0 7803 0593 0/92/$3.00
Conference Sponsor: IEEE
Conference Date: 10-13 May 1992 Conference Location: San Diego, CA, USA
Language: English
Subfile: B C

...Abstract: used to store one or more full size images, typically the

VGA standard 640*480 **pixel** range, with **many** other supported formats available. It also serves as a RAM buffer permitting random access of...
... images, typically by accessing and rewriting 64*64 pixel blocks in the graphics processor's **frame buffer** .
...Identifiers: **frame buffer**

43/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

02596867 INSPEC Abstract Number: B86011483, C86008956
Title: Super Buffer: systolic VLSI graphics engine for real time raster image generation
Author(s): Gharachorloo, N.; Pottle, C.
Author Affiliation: Sch. of Electr. Eng., Cornell Univ., Ithaca, NY, USA
Conference Title: 1985 Chapel Hill Conference on Very Large Scale Integration p.285-305
Editor(s): Fuchs, H.
Publisher: Computer Science Press, Rockville, MD, USA
Publication Date: 1985 Country of Publication: USA xiii+476 pp.
ISBN: 0 88175 103 0
Conference Sponsor: NSF; Univ. North Carolina
Conference Date: 1985 Conference Location: Chapel Hill, NC, USA
Language: English
Subfile: B C

...Abstract: s point of view, the simplest system in the family behaves as an extremely fast **frame buffer** . More advanced systems have the capability of real time hidden surface removal and polygon shading...

... identical specialized Pixel Processors which collaborate to break the real time computation barrier by performing **several** billion **pixel** operations per second in order to generate raster images in real time. The general purpose...
...Identifiers: **frame buffer** ;

43/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02459300 INSPEC Abstract Number: C85028668
Title: A general-purpose multi-microprocessor raster graphics display system with anti-aliasing
Author(s): Piller, E.
Author Affiliation: Tech. Univ. Wien, Austria
Journal: Computer Graphics Forum vol.4, no.1 p.33-41
Publication Date: Jan. 1985 Country of Publication: Netherlands
CODEN: CGFODY ISSN: 0167-7055
Language: English
Subfile: C

...Abstract: device contains a processor for the application program, two dedicated processors and two separate identical **frame buffers** , each of them containing one whole set of image data. Applying algorithms for anti-aliasing, virtual pixel dislocation (intensity dislocation) and **multi - pixel** -overlappings with hidden line (surface) elimination the image readability and quality can be increased considerably...
...Identifiers: **frame buffers** ;

43/3,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01815521 INSPEC Abstract Number: C82011852
Title: A frame buffer **system with enhanced functionality**
Author(s): Crow, F.C.; Howard, M.W.
Author Affiliation: Ohio State Univ., Columbus, OH, USA
Journal: Computer Graphics vol.15, no.3 p.63-9
Publication Date: Aug. 1981 Country of Publication: USA
CODEN: CGRADI ISSN: 0097-8930
Conference Title: SIGGRAPH'81. Eighth Annual Conference on Computer Graphics and Interactive Techniques
Conference Sponsor: ACM
Conference Date: 3-7 Aug. 1981 Conference Location: Dallas, TX, USA
Language: English
Subfile: C

Title: A frame buffer **system with enhanced functionality**
Abstract: A video-resolution **frame buffer** system with 32 bits per pixel is described. The system includes, in addition to standard...

... zoom and pan, an arithmetic unit at the update port which allows local computation of **many** frequently-used **pixel** -level functions combining stored pixel values with incoming pixel values. In addition to the standard ...
...Identifiers: **frame buffer** system...

...video-resolution **frame buffer** system

43/3,K/6 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1592644 NTIS Accession Number: AD-A236 631/8
Efficient Supersampling Antialiasing for High-Performance Architectures
Molnar, S.
North Carolina Univ. at Chapel Hill. Dept. of Computer Science.
Corp. Source Codes: 045592060; 409668
Report No.: TR91-023
Apr 91 23p
Languages: English
Journal Announcement: GRAI9120
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01

... of supersampling antialiasing in high-performance graphics architectures. The traditional approach is to sample each **pixel** with **multiple** , regularly spaced or jittered samples, and to blend the sample values into a final value...

... can be implemented on any high-performance system that point samples accurately and has sufficient **frame - buffer** storage for two color buffers.

43/3,K/7 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1479248 NTIS Accession Number: AD-A215 017/5
Near Real-Time CSG (Constructive Solid Geometry) Rendering Using Tree Normalization and Geometric Pruning
Goldfeather, J. ; Molnar, S. ; Turk, G. ; Fuchs, H.
North Carolina Univ. at Chapel Hill.
Corp. Source Codes: 045592000; 259500
May 89 9p
Languages: English Document Type: Journal article
Journal Announcement: GRAI9006
Pub. in IEEE Computer Graphics and Applications, v9 n3 p20-28 May 89.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01

... describes a set of algorithms for efficiently rendering a CSG-defined object directly into a **frame buffer** without converting first to a boundary representation. This method requires only that the **frame buffer** contain sufficient memory to hold two color values, two depth values, and three one-bit...
... attain similar speeds on many of the next-generation high-performance graphics systems that have **frame buffers** with **many** bits per **pixel** . Reprints. (jhd)

43/3,K/8 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

1004389 NTIS Accession Number: AD-A122 104/3
Architectures and Algorithms for Parallel Updates of Raster Scan Displays
(Doctoral thesis)
Gupta, S.
Carnegie-Mellon Univ., Pittsburgh, PA. Dept. of Computer Science.
Corp. Source Codes: 005343001; 403081
Report No.: CMU-CS-82-111
Dec 81 174p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8308
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A08/MF A01

The **frame buffer** memory organization is the key to achieving high display performance. Traditional **frame buffer** designs use the scan-line organization which allows **several pixels** along the length of a scan-line to be updated together. This thesis advocates the...
... uses one custom designed LSI chip, 64 copies of which are required to implement the **frame buffer** memory system. (Author)

43/3,K/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02832746 E.I. Monthly No: EI8912127317
Title: Transparency and antialiasing algorithms implemented with the virtual pixel maps technique.
Author: Mammen, Abraham
Corporate Source: Stellar Computer, Newton, MA, USA
Source: IEEE Computer Graphics and Applications v 9 n 4 Jul 1989 p 43-55
Publication Year: 1989
CODEN: ICGADZ ISSN: 0272-1716
Language: English

...Abstract: pixel maps technique in the support of high-quality rendering operations are described. A dedicated **frame buffer** with a fixed number of bits per pixel is inappropriate for implementing high-quality rendering...
Identifiers: ANTIALIASING ALGORITHMS; VIRTUAL PIXEL MAPS TECHNIQUE; MULTIPASS TRANSPARENCY; **MULTIPLE PIXEL** VISIT PROBLEM

43/3,K/10 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01218085 ORDER NO: AAD92-11316
A GENERAL PURPOSE RASTERIZATION PROCESSOR (RISC)
Author: ZOULAS, CHRISTOS STAMOULIS
Degree: PH.D.
Year: 1992
Corporate Source/Institution: CORNELL UNIVERSITY (0058)
Source: VOLUME 52/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 6585. 164 PAGES

...high end systems.
In contrast with current rasterization systems which are bound to a specific **frame - buffer** architecture SRP's can be configured in parallel in different ways depending on the memory architecture of the **frame - buffer** and the cost/performance requirements.
The general purpose nature of the RISC processor allows for arbitrary rasterization primitives, while the pixel unit can operate independently for **multiple pixels** . Taking advantage of the features of each unit, the SRP processor can be used to...

43/3,K/11 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01134072 ORDER NO: AADD--90581
A CONCURRENT PROCESSING SYSTEM FOR THE GENERATION OF REAL-TIME THREE-DIMENSIONAL GRAPHICS: A VME-BUS COMPATIBLE LOW COST RASTER GRAPHICS SYSTEM FOR THE GENERATION OF POLYGONALLY MODELLED THREE-DIMENSIONAL IMAGES IN REAL-TIME
Author: ALI, FAKHRALDEEN H.
Degree: PH.D.
Year: 1989
Corporate Source/Institution: UNIVERSITY OF BRADFORD (UNITED KINGDOM) (0401)

Source: VOLUME 51/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3449. 347 PAGES

...image generation on a raster scan display requires rapid writing to and reading from a **frame buffer** . This thesis presents a graphics system which is capable of generating images of three-dimensional...

...units. A scan-conversion unit which is designed around a dedicated graphics processor driving a **frame buffer** memory. This unit is capable of writing **multiple pixels** into the **frame buffer** in less than 15 nanoseconds per pixel. The second unit consists of four microcomputer boards...
?

44/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

00038416 INSPEC Abstract Number: B69010772, C69005919
Title: Magnetic memory employing stress wave
Inventor(s): Shohbender, R.
Assignee(s): Radio Corp. America
Patent Number: US 3411149 Issue Date: 681112
Application Date: 640904
Priority Appl. Number: US 394545
Country of Publication: USA
Language: English
Subfile: B C

Abstract: A memory **array** comprising a plurality of **rows** of thin film magnetic memory elements, means to propagate a sonic stress wave through any selected one of said **rows** of memory elements, said memory elements in each **row** being closely spaced so that said sonic stress wave spans a plurality of memory elements...

...elements spanned by a sonic stress wave, each of said conductors linking a plurality of **nonadjacent** memory elements in one **row** which are sufficiently spaced from each other so that only one memory element in the **row** is stressed at a time, each conductor also linking corresponding memory elements of all other **rows** , means to energize each of said electrical **stored** in the memory elements, and a plurality of sense conductors with bit-serial information signals...

... wave passing through memory elements linked by the conductor along any selected one of said **rows** , whereby information is **stored** in the memory elements, and a plurality of sense amplifiers each coupled to one of said electrical conductors to receive **stored** information in the form of bit-serial information signals induced on the electrical conductor in response to the propagation of a sonic stress wave through any selected one of the **rows** of memory elements.
Descriptors: magnetic film **stores** ;
?

```
File 344:Chinese Patents Abs Aug 1985-2004/Mar
         (c) 2004 European Patent Office
File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
         (c) 2004  Thomson Derwent

Set     Items   Description
S1          2   SENSE(3N)AMPLIFIER? AND (SHARED OR USED)(3N)(ADJACENT? OR -
             ADJOIN?)(3N)ARRAY?
S2        432   (INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN?)(3N)MEMORY AND C-
             ONTROLLER(3N)(IC OR INTEGRATED()CIRCUIT? OR CHIP?? OR CIRCUIT-
             ??)
S3          0   (STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT
             OR PLACING)(3N)(ROW?? OR LINE?)(3N)(NONADJOIN? OR NONADJACENT?
              OR NON-ADJACEN?)(3N)ARRAY?
S4     437575   VIDEO
S5      11831   (PLURAL? OR MANY OR SEVERAL OR NUMEROUS OR MANY OR MULTI OR
              MULTIPLE)(3N)(PIXEL? OR PEL OR PICTURE()ELEMENT? OR PICTURE(-
             3N)CELL??)
S6      19219   HORIZONTAL(3N)LINE?
S7     110576   IMAGE(3N)DISPLAY?
S8      50243   (FIRST OR SECOND OR TWO OR 2 TOP OR BOTTOM)(3N)(HALF OR HA-
             LVES)
S9        289   (EVEN OR ODD)(3N)NUMBER?(3N)ARRAY?
S10      4934   FRAME(3N)BUFFER?
S11       266   PROCESSOR? AND (TRACK? OR MONITOR? OR DETECT? OR DETERMIN?)
              AND (ACTIVE OR OPEN OR OFF) AND ARRAY??
S12   1196645   IC=(G11C? OR G06F?)
S13         3   (STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT
             OR PLACING) AND (ROW?? OR LINE?) AND (NONADJOIN? OR NONADJACE-
             NT? OR NON-ADJACEN?) AND ARRAY?
S14       322   AMPLIFIER? AND (SHAR? OR USING OR USE OR USED) AND (ADJACE-
             NT? OR ADJOIN?) AND ARRAY?
S15         1   S2 AND S14
S16         1   S15 NOT (S1 OR S13)
S17         0   S4 AND S10 AND S14
S18        18   (S4 OR S5) AND S14
S19         0   S18 AND S11
S20         0   S18 AND S2
S21         0   S18 AND S9
S22         0   S18 AND (EVEN OR ODD)(3N)NUMBER?
S23         4   S18 AND AD=19960809:19991231/PR
S24         1   S18 AND AD=20000101:20021231/PR
S25         0   S18 AND AD=20030101:20040329/PR
S26         4   S23 OR S24
S27        14   S18 NOT S26
S28        14   IDPAT (sorted in duplicate/non-duplicate order)
S29        14   IDPAT (primary/non-duplicate records only)
S30         2   S5 AND S2
S31         2   S30 NOT (S29 OR S13 OR S1 OR S15)
S32         0   S8 AND S9 AND S10
S33         0   S9 AND S10
S34         0   S7 AND S8 AND S9
```

1/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03268980 **Image available**
DYNAMIC TYPE SEMICONDUCTOR STORAGE DEVICE

PUB. NO.: 02-244480 [JP 2244480 A]
PUBLISHED: September 28, 1990 (19900928)
INVENTOR(s): TSUCHIDA KENJI
OWAKI YUKITO
WATANABE SHIGEYOSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-063807 [JP 8963807]
FILED: March 17, 1989 (19890317)
JOURNAL: Section: P, Section No. 1144, Vol. 14, No. 569, Pg. 128, December 18, 1990 (19901218)

ABSTRACT
... the chip size and to reduce the power consumption by using in common an NMOS **sense** **amplifier** and a PMOS **sense** **amplifier** by a sub-cell array, and providing an equalizing circuit on a block selecting circuit...

...CONSTITUTION: A PMOS **sense** **amplifier** 131 for amplifying a high potential side is placed in one end part of its...

...cell array 111 through block selection MOS transistors QP11, QP12 of (p) channel, an NMOS **sense** **amplifier** 12 for amplifying a low potential side is placed in the other end part of...

...cell array 111 through block selection MOS transistors QN11, QN12 of (n) channel, and the **sense** **amplifier** 131 between two **adjacent** sub-cell **arrays** 111, 112 is **used** in common by these two sub-cell arrays 111, 112. Also, an equalizing circuit is...

1/3,K/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012836722 **Image available**
WPI Acc No: 2000-008554/200001
XRPX Acc No: N00-007783
Bit-line equalizer sharing circuit of DRAM - selects any one of cell array based on predetermined control instruction and bit-line potential transmittance
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11288600	A	19991019	JP 9887381	A	19980331	200001	B

Priority Applications (No Type Date): JP 9887381 A 19980331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11288600	A		15	G11C-029/00	

...Abstract (Basic): A share unit comprising DQ gate circuit (DQC) that performs relationship to input-output of **sense** **amplifier** circuit

(S/A), equalizer circuit (EQ) of bit-line pair, is provided between right and...

...ADVANTAGE - Shortens testing time of memory, since the bit- line equalizer circuit is **shared** between **adjacent** cell **array** for performing screening of inferior equalizer effectively. DESCRIPTION OF DRAWING(S) - The figure shows circuit...

...ARY-R,ARY-L) Cell arrays; (DQC) DQ gate circuit; (EQ) Equalizer circuit; (S/A) **Sense** **amplifier** circuit; (Tr1L,Tr2L,Tr1R,Tr2R) Gate circuits ...

?

13/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009960781 **Image available**
WPI Acc No: 1994-228494/199428
XRPX Acc No: N98-014483
Designing layout of large scale LSI integrated circuit - placing **each cell of second group of cells at open spaces of first group of cells placed in** array **form so as to make layout of LSI rectangular**
Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)
Inventor: HAYASHI E; MIYAMOTO H; TABIRA Y
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6163699	A	19940610	JP 93194616	A	19930805	199428	B
US 5694328	A	19971202	US 93102616	A	19930805	199803	
			US 96631904	A	19960412		
JP 3115743	B2	20001211	JP 93194616	A	19930805	200101	

Priority Applications (No Type Date): JP 92210028 A 19920806
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6163699	A		7	H01L-021/82	
US 5694328	A		13	G06F-017/50	Cont of application US 93102616
JP 3115743	B2		7	H01L-021/82	Previous Publ. patent JP 6163699

... placing **each cell of second group of cells at open spaces of first group of cells placed in** array **form so as to make layout of LSI rectangular**

...Abstract (Basic): are divided into a number of groups of cells. The cells are placed in an **array** form at positions which are either adjacent or **nonadjacent** .
...

...substantially rectangular or square. Power buses are routed parallel to each other, and power supply **lines** are routed from the power buses to cells. Data **lines** are routed between the terminals of the cells...

...minimum size when designing cells, and total laid out block size also is smaller. Data **lines** between cells are routed using input terminals and output terminals on four sides of the cells. This makes the data **line** capacity and resistance optimum, and makes the data **line** delay smaller
...Title Terms: **PLACE** ;

13/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007534099 **Image available**
WPI Acc No: 1988-168031/198824
XRPX Acc No: N88-128391
Periodic matrix line **or dot space measuring method - having scanned space data** stored **in columns with column average calculated to obtain average space length**
Patent Assignee: RCA LICENSING CORP (RADC)
Inventor: KRUFKA F S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4748330	A	19880531	US 86944525	A	19861222	198824	B

Priority Applications (No Type Date): US 86944525 A 19861222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4748330	A		24		

Periodic matrix line **or dot space measuring method...**

...**having scanned space data** stored **in columns with column average calculated to obtain average space length**

...Abstract (Basic): The matrix space measuring method involves **placing** the matrix between an energy source and an **array** of pixel for receiving the energy from the matrix and irradiating the matrix with the energy and scanning a number of image **lines** from the matrix across the **array** and producing signals representative of the spaces and areas between. The signals are converted into...

...data values are transmitted to a memory storing the values for each of the scan **lines** as a **row** and for successive scan **lines** as columns ...

...Selected data values in predetermined groups of columns representing corresponding **nonadjacent** spaces of the periodic matrix are added to obtain a total for each group. The...

...value for each group. The average data value for each group is multiplied by a **linear** value representing the length of each pixel to obtain the average space length for each...
...Title Terms: **LINE** ;

13/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007522645
WPI Acc No: 1988-156578/198823
XRAM Acc No: C88-069805
Textiles for reinforcement of injection moulded resins - with continuous interstitial passages to facilitate impregnation
Patent Assignee: BROCHIER SA (BROC-N)
Inventor: AUCAGNE J; BOMPARD B; LAPRESLE B
Number of Countries: 016 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 270411	A	19880608	EP 87402479	A	19871103	198823	B
EP 270411	B	19901114				199046	
DE 3766228	G	19901220				199101	
ES 2019397	B	19910616				199129	
CA 1331946	C	19940913	CA 551003	A	19871104	199437	
JP 95081224	B2	19950830	JP 87278448	A	19871105	199539	
US 5484642	A	19960116	US 87117093	A	19871105	199609	
			US 89408460	A	19890915		
			US 92965519	A	19921023		

Priority Applications (No Type Date): FR 8615425 A 19861105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 270411	A	F	13		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
EP 270411	B				
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
CA 1331946	C	F		D03D-001/00	
JP 95081224	B2		8	D03D-001/00	Based on patent JP 63203844
US 5484642	A		9	B32B-003/00	Cont of application US 87117093
					Cont of application US 89408460

...Abstract (Basic): of the yarns, and/or in their sizes and/or twists. The passages may be **linear** or curved, mutually parallel or not. The yarns may be preimpregnated. The fabrics may incorporate both knitted and woven layers. **Arrays** of individual yarns may be interposed between layers of fabric, to enhance interfacial flow of...

...mouldings incorporated several (e.g. ten) layers of fabric, to combine through impregnation, and hence **strong** mechanical properties, for e.g. aeronautical applications, with the relative short production cycle times associated...

...Abstract (Equivalent): of the yarns, and/or in their sizes and/or twists. The passages may be **linear** or curved, mutually parallel or not. The yarns may be preimpregnated. The fabrics may incorporate both knitted and woven layers. **Arrays** of individual yarns may be interposed between layers of fabric, to enhance interfacial flow of...

...mouldings incorporated several (e.g. ten) layers of fabric, to combine through impregnation, and hence **strong** mechanical properties, for e.g. aeronautical applications, with the relative short production cycle times associated...

...Abstract (Equivalent): the substantially round threads have been formed from substantially flat multifilament threads helically wrapped in **nonadjoining** turns with an additional thread, and (2) the substantially round threads are uniformly distributed in...

?

16/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007602446
WPI Acc No: 1988-236378/198834
XRPX Acc No: N88-179622
CMOS dynamic random access memory - has switch device for interconnecting divided bit line pairs between memory cell array **blocks**
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: MIYAMOTO H; YAMADA M
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 278155	A	19880817	EP 87308853	A	19871006	198834	B
US 5053997	A	19911001	US 87132646	A	19871208	199142	
EP 278155	B1	19920722	EP 87308853	A	19871006	199230	
DE 3780621	G	19920827	DE 3780621	A	19871006	199236	
			EP 87308853	A	19871006		

Priority Applications (No Type Date): JP 8728782 A 19870210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 278155	A	E	29		
Designated States (Regional): DE FR GB					
EP 278155	B1	E	26	G11C-011/401	
Designated States (Regional): DE FR GB					
DE 3780621	G			G11C-011/401	Based on patent EP 278155

... **has switch device for interconnecting divided bit line pairs between memory cell** array **blocks**

...Abstract (Basic): The **memory** **includes** a number of **memory** cell **array** blocks with each block having a number of word lines and a number of bit...

...line pairs and to one of the word lines. A potential difference amplifying device is **used** on the divided bit line pair so that one divided bit lines is at a...

...A switching device interconnects the divided bit line pairs between the **adjacent** memory cell **array** blocks. A timing controller device is coupled to the equalising device for controlling the equalising device selectively and at different times among the memory cell **array** blocks ...

... **USE** /ADVANTAGE - Providing high speed dynamic RAM with large operating margins. Prevents potentials of part of
...Abstract (Equivalent): Each bit line pair has a number of divided bit line pair sections. A sense **amplifier** amplifies a potential difference of each the divided bit line pair section so that one...

...equaliser of each divided bit line pair section prior to a sensing operation. The timing **controller** has a **circuit** for continuing equalisation of a first divided bit line pair section of a given bit...

... **USE** - In computer systems.
...Title Terms: **ARRAY** ;
?

29/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013912245 **Image available**
WPI Acc No: 2001-396458/200142
Related WPI Acc No: 2000-222287
XRPX Acc No: N01-292014
Spectacles with telescope array , **has telescopes with front convex surface and back concave surface, arranged** adjacent **to each other with each convex surface facing the same direction**
Patent Assignee: UNIV LOUISIANA STATE & AGRIC & MECH COLL (LOUU)
Inventor: FELDMAN M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6226120	B1	20010501	US 94347804	A	19941130	200142	B

Priority Applications (No Type Date): US 94347804 A 19941130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6226120	B1		18	G02B-023/00	

Spectacles with telescope array , **has telescopes with front convex surface and back concave surface, arranged** adjacent **to each other with each convex surface facing the same direction**

Abstract (Basic):
... Each telescope in **array** comprises a front convex surface of 0.1 mm diameter and a back concave surface...

...telescope are held together with their axes parallel to each other, and convex surfaces of **adjacent** telescopes face same direction. Each **array** comprises opaque regions between telescopes to inhibit light from **adjacent** telescope.
... a) **Video** display and optical telescope combination...

... **USE** - ...

...Spectacles with telescope **array** for viewing initially dim visible light image...

...Alignment of the eye is not critical with this telescope **array** , since the viewer looks through several telescopes simultaneously with each eye. Telescope **arrays** are not bulky, may be handheld like a magnifying glass or fitted to a frame like eye glasses. The telescope in the **array** are diffraction limited near the optical axis and have negligible light loss, hence images are **sharp** and bright...

...The figure shows an **array** of micro-telescope in combination with an electronic **amplifier** and a **video** display
Technology Focus:
... The telescope **array** is formed of polymethylmethacrylate (PMMA) resist.
...Title Terms: **ARRAY** ;

29/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012519758 **Image available**
WPI Acc No: 1999-325864/199927
XRPX Acc No: N99-244377
Dual-line reading single chip MOS image sensor in video **cameras**
Patent Assignee: OMNIVISION TECHNOLOGIES INC (OMNI-N)
Inventor: CHEN D; HE X; SHYU T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5901257	A	19990504	US 96642537	A	19960503	199927	B
TW 333712	A	19980611	TW 96113729	A	19961109	199927	

Priority Applications (No Type Date): US 96642537 A 19960503
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5901257	A		15	G06K-007/00	
TW 333712	A			H01L-027/48	

Dual-line reading single chip MOS image sensor in video **cameras**

Abstract (Basic):
... store amplified pixel signals (P1-P4). Switches (SW1) selectively assign pixel signals from a pixel **array** row (101) on capacitors (C1,C2). Switches (SW2) selectively assign pixel signals from **adjacent** pixel **array** row (101) on capacitors (C3-C4). Switches (SW3,SW4) selectively reads out pixel signals onto...
... stored on capacitors (C1-C4). The line signals (SIG1,SIG2) are amplified by a charge **amplifier** (305) and become amplified line signals (SIG1',SIG2'). The pixel **array** includes a single column of pixels (103), designated as pixels (103A-103D). A color filter pattern with green, yellow and cyan filters is superimposed on the pixel **array** .
...

...1) the method of reading a color image sensor having pixel **array** , and
...

... **USE** - ...

...In computers, control systems, telecommunications and **video** cameras...

... **Use** of an external delay line device is eliminated since the line signals are simultaneously read from **adjacent** rows of pixels...

...Pixel **array** (101...

...Charge **amplifier** (305
...Title Terms: **VIDEO** ;

29/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011582759 **Image available**
WPI Acc No: 1997-559240/199751
XRPX Acc No: N97-466062
High resolution flat panel for radiation imaging with compensation circuit - has multiple **pairs of** adjacent pixels **in each row of**

array **that** share **source lines leading to charge** amplifiers **for sensing signal charges**

Patent Assignee: IFIRE TECHNOLOGY INC (IFIR-N); 1294339 ONTARIO INC (ONET-N); LITTON SYSTEMS CANADA LTD (LITO); HUANG Z S (HUAN-I)

Inventor: HUANG Z S

Number of Countries: 020 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9742661	A1	19971113	WO 96CA294	A	19960508	199751	B
EP 897597	A1	19990224	EP 96913400	A	19960508	199912	
			WO 96CA294	A	19960508		
JP 2000512804	W	20000926	WO 96CA294	A	19960508	200051	
			JP 97539364	A	19960508		
US 6232607	B1	20010515	WO 96CA294	A	19960508	200129	
			US 98180091	A	19981102		
US 20020053946	A1	20020509	WO 96CA294	A	19960508	200235	
			US 98180091	A	19981102		
			US 2001809376	A	20010315		
EP 897597	B1	20020911	EP 96913400	A	19960508	200264	
			WO 96CA294	A	19960508		
DE 69623659	E	20021017	DE 623659	A	19960508	200276	
			EP 96913400	A	19960508		
			WO 96CA294	A	19960508		
US 6486470	B2	20021126	WO 96CA294	A	19960508	200281	
			US 98180091	A	19981102		
			US 2001809376	A	20010315		

Priority Applications (No Type Date): WO 96CA294 A 19960508

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9742661	A1	E	33	H01L-027/146	
Designated States (National): CA JP US					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 897597	A1	E		H01L-027/146	Based on patent WO 9742661
Designated States (Regional): DE FR GB NL					
JP 2000512804	W		33	H01L-027/14	Based on patent WO 9742661
US 6232607	B1			H01L-031/02	Based on patent WO 9742661
US 20020053946	A1			H03G-003/00	Div ex application WO 96CA294
					Div ex application US 98180091
EP 897597	B1	E		H01L-027/146	Based on patent WO 9742661
Designated States (Regional): DE FR GB NL					
DE 69623659	E			H01L-027/146	Based on patent EP 897597
					Based on patent WO 9742661
US 6486470	B2			H01L-027/146	Div ex application WO 96CA294
					Div ex application US 98180091
					Div ex patent US 6232607

... **has** multiple **pairs of** adjacent pixels **in each row of** array **that** share **source lines leading to charge** amplifiers **for sensing signal charges**

...Abstract (Basic): The panel includes gate lines (24) which interconnect rows of pixels (22) in an **array** while source lines (26) interconnect columns. Gate drivers (28) provide successive pulses to the gate...

...The source lines lead to charge **amplifiers** (32) sensing signal charges stored by selected pixels. At least one pair of **adjacent** pixels in each row **shares** a source line. Gating of each pair is controlled by control logic ensuring that only one of the stored charges is applied

to a **shared** source line at a time...

... **USE** - For medical x-ray imaging system...

...ADVANTAGE - Reduces number of charge **amplifiers** required while maintaining high resolution

...Title Terms: **ADJACENT** ;

29/3,K/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010829364 **Image available**

WPI Acc No: 1996-326316/199633

XRPX Acc No: N96-274827

Semiconductor memory such as video **random access memory - has potential switching circuit that is** used **to set potential of output node as bit line pre-charge potential for initial set up potential or predetermined standard potential**

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: KAI Y

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8147965	A	19960607	JP 94280418	A	19941115	199633	B
US 5650970	A	19970722	US 95533718	A	19950926	199735	
KR 184088	B1	19990415	KR 9541470	A	19951115	200048	
CN 1153983	A	19970709	CN 95119241	A	19951114	200368	

Priority Applications (No Type Date): JP 94280418 A 19941115

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8147965	A		9	G11C-011/401	
US 5650970	A		16	G11C-007/00	
KR 184088	B1			G11C-007/00	
CN 1153983	A			G11C-011/34	

Semiconductor memory such as video **random access memory**...

...**has potential switching circuit that is** used **to set potential of output node as bit line pre-charge potential for initial set**...

...Abstract (Basic): The semiconductor memory consists of several sub-circuits. The bit line pair of memory cell **array** is divided as first and second bit line pairs through the transfer gates (CS), for...

...The pre-charge equalizer circuit (10) is located on one side of the memory circuit **adjacent** to the sense **amplifiers** (11,12). The flash write control circuit (15) performs the switching control of the first ...

...ADVANTAGE - Does not increase circuit scale of memory **array** . Simplifies circuit composition...

...Abstract (Equivalent): a memory cell **array** having memory cells of dynamic type arranged in rows and columns...

...a plurality of bit line potential sense **amplifiers** , each of the bit line potential sense **amplifiers** being connected to the second portion of one of the bit line pairs, and being...

...of the output node to one of a bit line pre-charge potential, which is **used** to set an initial bit line potential, and a predetermined reference potential...
...Title Terms: **VIDEO ;**

29/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010133949 **Image available**
WPI Acc No: 1995-035200/199505
XRPX Acc No: N95-027790
Broadband space-time signals communication system - has antenna arrays **made of different electrical lengths with** adjacent **elements at spacing of half wavelength**
Patent Assignee: MILITARY COMMUNIC ACAD (MILI-R)
Inventor: DOLMATOV A V; KONOVALOV L M; PRIVALOV A A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RU 2013013	C1	19940515	SU 5015956	A	19910720	199505	B

Priority Applications (No Type Date): SU 5015956 A 19910720
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RU 2013013	C1		6	H04L-005/02	

... **has antenna** arrays **made of different electrical lengths with** adjacent **elements at spacing of half wavelength**
...Abstract (Basic): pseudo-random series generator (3), synchronisers (4,17), modulator (5), carrier frequency oscillator (6), power **amplifier** (7), controlled commutators (8,12), spatial phase-keyed pseudo-random series shapers (9,13) transmitting antenna (10), receiving antenna (11), mixer (14), heterodyne (15), i.f. **amplifier** (16), matching filter (18), resolving unit (19) and data receiver (20). Appts. now has a...

...phase-keyed signal from generator (3) on its other input. This is a series of **video** pulses of width tn!=T/k, where k is the no. of pulses and T...

... **USE** /ADVANTAGE - Appts. is concerned with radio and may be **used** in radio communications. Bul.9/15.5.94
...Title Terms: **ARRAY ;**

29/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010073415 **Image available**
WPI Acc No: 1994-341128/199442
XRPX Acc No: N94-267595
Single gun beam index colour CRT index signal generating system in e.g. work-station or television - synchronises CRT video **output with index strips overlying red, blue and green phosphor strips, and index strips for each colour connected in three parallel** arrays **, so that pulses are triggered for** video **modulation**

Patent Assignee: SMITH C E (SMIT-I); WRITER P L (WRIT-I); NUSBAUM H (NUSB-I); ZACCARDO C F (ZACC-I); ZACCARO C F (ZACC-I)
Inventor: SMITH C E; WRITER P L
Number of Countries: 042 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5359266	A	19941025	US 92978934	A	19921120	199442	B
WO 9525338	A1	19950921	WO 94US2785	A	19940315	199543	N
AU 9469029	A	19951003	AU 9469029	A	19940315	199602	N
			WO 94US2785	A	19940315		

Priority Applications (No Type Date): US 92978934 A 19921120; WO 94US2785 A 19940315; AU 9469029 A 19940315
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9525338	A1		20	H01J-029/52	

Designated States (National): AU BB BG BR CA CN CZ FI HU JP KR KZ LK MG MN MW NO NZ PL RO RU SD SK UA
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 9469029	A			H01J-029/52	Based on patent WO 9525338
US 5359266	A			H01J-029/52	

... **synchronises CRT** video **output with index strips overlying red, blue and green phosphor** strips, and index strips for each colour connected in **three parallel** arrays **, so that pulses are triggered for** video **modulation**

...Abstract (Basic): three, with strips of conductive or photovoltaic material overlaying each phosphor strip, or placed between **adjacent** strips. The same colour conductive strips are connected in parallel in three **arrays ,** and connected to three individual trigger buses. The conductive lines are connected to a positive...

...trigger pulses are generated in the conductive strips and are fed to a trigger pulse **amplifier** and then to a multiplexer and **used** as control signals. The multiplexer in turn gates the colour **video** signals from a remote source, so that the corresponding **video** signal for that colour is modulating the beam as the electron beam strikes a phosphor...

... **USE** /ADVANTAGE - E.g. direct view and projection HDTV. Larger screen size, increased resolution and brightness
...Title Terms: **VIDEO ;**

29/3,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009496054 **Image available**
WPI Acc No: 1993-189590/199324
XRPX Acc No: N93-145704
Dual port memory e.g. for video **RAM in personal computer etc. - has transfer switches between bit lines and serial register and between bit lines and divided sense** amplifier **, controlled by internal signals**
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC KK (MITQ)
Inventor: FUDEYASU Y; INOUE K
Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4222273	A1	19930609	DE 4222273	A	19920707	199324	B
US 5325329	A	19940628	US 92887253	A	19920522	199425	
DE 4222273	C2	19941110	DE 4222273	A	19920707	199443	
KR 9601778	B1	19960205	KR 9221351	A	19921113	199908	

Priority Applications (No Type Date): JP 91319226 A 19911203

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4222273	A1		31	G11C-007/00	
US 5325329	A		30	G11C-011/54	
DE 4222273	C2		29	G11C-007/00	
KR 9601778	B1			G11C-007/00	

Dual port memory e.g. for video **RAM in personal computer etc...**

...**transfer switches between bit lines and serial register and between bit lines and divided sense** amplifier , **controlled by internal signals**

...Abstract (Basic): The dual port memory includes a sense **amplifier** (1200a, b) between two **adjacent** blocks (1100a, b) for amplifying data for a line, read-out from one block or written into it. A second memory **array** (1300) contains numerous memory cells (310) in a line. A transmitter acts on data for a line between the two memory **arrays** .
...

...The blocks in both **arrays** are arranged in a common column. The transmitter contains numerous bit lines (2000) intersecting any arbitrary block. A first transmit control (2200a, b) operates between the **amplifier** and the bit lines, while a second transmit control (2100a, b) operates between the bit lines and the second memory **array** .

...Abstract (Equivalent): A two-channel memory described has a first memory **array** divided into a number of blocks (1100a, 1100b, 1100c, 1100d)contains a number of memory cells arranged in rows and columns, and a number of amplifies (1200a, 1200b) between **adjacent** block for amplifying row data read from a block or row data to be entered...

...A second memory **array** (1300) contains a number of memory cells arranged in a row and a unit transmits data for a row between the first memory **array** and the second memory **array** .The blocks of the first memory **array** and the second memory **array** are arranged in a common column, while the transmitting unit has a number of lines...

...blocks and also units (2100a, 2100b, 2200a, 2200b) for controlling the data transmission between the **amplifiers** and the lines, the lines and the second **array** .
...

... **USE** /ADVANTAGE - Personal computers . Facilitates transmission of data from one memory **array** to another

...Abstract (Equivalent): The dual port memory comprises a first memory **array** including memory cells arranged in rows and columns, and divided into blocks. An **amplifier** includes sense **amplifiers** disposed between **adjacent** blocks for amplifying data for one row read from any block, to be written to any other block. A second memory **array** includes memory cells arranged in one row, and a transfer unit for transferring data for one row between the first memory **array** and

second memory **array** .
...

...The blocks in the first memory **array** and second memory **array** are arranged in a common column, and the transfer unit includes transfer lines arranged so as to cross any block with each sense **amplifier** connected to a single transfer line. A first transfer control controls transfer of data between the **amplifier** transfer lines, and a second transfer control controls transfer of data between the transfer lines and the second memory **array** .

...Title Terms: **VIDEO** ;

29/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009385024
WPI Acc No: 1993-078502/199310
XRPX Acc No: N93-060232
Dual port memories for colour look-up table - has video **port and path for reading data identifying colours for pixels at greater than 100 or even greater than 200 megahertz with CPU port and path for reading and writing data at memory**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: PLANTS W; RUNALDUE T J
Number of Countries: 001 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 530988	A2	19930310	EP 92307281	A	19920810	199310	B
US 5325338	A	19940628	US 91754910	A	19910904	199425	
EP 530988	A3	19950614	EP 92307281	A	19920810	199610	
US 5576560	A	19961119	US 91754910	A	19910904	199701	
			US 94267036	A	19940627		

Priority Applications (No Type Date): US 91754910 A 19910904; US 94267036 A 19940627
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 530988	A2	E	27	G11C-011/407	
US 5325338	A		20	G11C-007/00	
US 5576560	A		21	H01L-027/10	Div ex application US 91754910
					Div ex patent US 5235338
EP 530988	A3			G11C-011/407	

... **has** video **port and path for reading data identifying colours for pixels at greater than 100 or...**

...Abstract (Basic): word lines connected to communicate data to and from the second access path. In an **array** of memory cells, each memory cell in a subset of the **array** includes a single ended port connected to one bit line and a word line in...

...A single ended sense **amplifier** is connected to the single ended port of one of the memory cells to receive...

... **USE** /ADVANTAGE - For display system. Has access path for reading data identifying colours for picture elements
...Abstract (Equivalent): On an integrated circuit, a circuit **including** a

first memory cell having a left edge, a right edge, an upper edge, and a lower edge and having an upper part **adjacent** to said upper edge and a lower part **adjacent** to said lower edge, wherein the first memory cell comprises...

...a substrate of **a** first doping type...

...a well of a second doping type **located** in said lower part of said memory cell;

...

...a first region and a **second** region of the second doping type, said first region extending to the left and upper...The integrated circuit memory has a **video** port and path for reading data identifying colours for pixels at greater than 100 or...

...CPU path, and a gate coupled to a word line of the CPU path. The **video** port includes an isolated sensing terminal and two transistors...

...the isolated sensing terminal, a second channel terminal coupled to a bit line of the **video** path, and a gate coupled to a word line of the **video** path...

... **USE** - For image display system
...Title Terms: **VIDEO** ;

29/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008954303 **Image available**
WPI Acc No: 1992-081572/199211
XRPX Acc No: N92-061207
Solid state image pick-up device - uses CCD having pair of horizontal registers and pilot signal generator
Patent Assignee: SONY CORP (SONY)
Inventor: KOBAYASHI A; ONGA M; SASE M; SATO Y; ONG
Number of Countries: 007 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 473966	A	19920311	EP 91113412	A	19910809	199211	B
JP 4096480	A	19920327	JP 90213485	A	19900809	199230	
JP 4096481	A	19920327	JP 90213484	A	19900809	199230	
US 5384596	A	19950124	US 91742004	A	19910808	199510	
			US 9339522	A	19930329		
			US 94238966	A	19940505		
EP 473966	B1	19960327	EP 91113412	A	19910809	199617	
DE 69118279	E	19960502	DE 618279	A	19910809	199623	
			EP 91113412	A	19910809		
KR 230468	B1	19991115	KR 9113747	A	19910809	200111	
SG 81892	A1	20010724	SG 968670	A	19910809	200151	

Priority Applications (No Type Date): JP 90213485 A 19900809; JP 90213484 A 19900809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 473966	A		11		
Designated States (Regional): DE FR GB					
JP 4096480	A		8	H04N-005/335	
JP 4096481	A		8	H04N-005/335	

US 5384596	A	9	H04N-005/335	Cont of application US 91742004
				Cont of application US 9339522
EP 473966	B1 E	11	H04N-003/15	

Designated States (Regional): DE FR GB

DE 69118279	E	H04N-003/15	Based on patent EP 473966
KR 230468	B1	H04N-005/335	
SG 81892	A1	H04N-003/15	

...Abstract (Basic): The pilot signal is inserted into a **video** signal without modifying the output signal timing by supplying the signal charges from the pilot...

...Abstract (Equivalent): imaging device in which a solid state image pickup unit including a photoelectric conversion element **array** for converting incident light is provided, and which comprises, - two horizontal registers (3a, 3b), two...

...Abstract (Equivalent): between the two circuit systems which is comprised of two correlated double sampling circuits, two **amplifiers** , two sample and hold circuits and a comparing circuit. The first correlated double sampling circuit, first **amplifier** , and first sample and hold circuit are connected in series between the output of the first horizontal register and the comparing circuit. The second double sampling circuit, second **amplifier** , and second sample and hold circuit are connected in series between the output of the...

...output of the comparing circuit connected to at least one of the first and second **amplifiers** to control its gain...

...The two horizontal registers each have an extended portion, the pilot signal generator being located **adjacent** the transfer side of the extended portions of the horizontal registers and supplying the pilot ...

... **USE** - CCD imaging system which prevents a horizontal stripe and flicker taking place due to a

29/3,K/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007942905 **Image available**

WPI Acc No: 1989-208017/198929

XRPX Acc No: N89-158640

Data reader for optical disk unit - uses operational amplifier **housed in optical head to amplify HF recorded data signals**

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: TAKEUCHI R

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3843621	A	19890713	DE 3843621	A	19881223	198929	B
US 5010541	A	19910423	US 88289128	A	19881223	199120	
DE 3843621	C	19911212				199150	

Priority Applications (No Type Date): JP 87330492 A 19871226

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3843621	A		8		

... **uses operational** amplifier **housed in optical head to amplify HF**

recorded data signals

...Abstract (Basic): disk surface to read and transmit data to a quadrant sensor (8). A photodiode sensor **array** (8) converts the optical signal to an electrical signal for division into high and low...

...A data processor (12) process L.F. components and transmits them back to an operational **amplifier** (A1) mounted on the optical head (3) for reconstitution as a **video** signal. A wideband signal is transmitted to a **video** circuit (19) for conversion to a **video** composite signal...

...L.F. signals (Vfs,Vts) from the processor (12) are **used** to focus and position a lens (6) via control units (15,16) and drive coils...

...ADVANTAGE - H.F. **amplifier** mounted **adjacent** to signal converter on head, therefore no spurious noise induced from cabling. No. L.F. **amplifier** on head, therefore head weight is reduced...

...Abstract (Equivalent): **USE** /ADVANTAGE - Reproduction of a high quality signal without the influence of noise. It is suitable

...Abstract (Equivalent): from the dividing element. Data from the optical disk is reproduced in response to the **amplifier** .

29/3,K/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007189583

WPI Acc No: 1987-186592/198727

XRPX Acc No: N87-139471

Solid-state image sensor with photoconductive cell array **- has signal detecting pre-** amplifier **connected to common electrodes through analog switches and load resistor**

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: ANBO K; NAKAI T; SHIMADA O; SUZUKI K

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 228023	A	19870708	EP 86117518	A	19861216	198727	B
JP 63012164	A	19880119	JP 86151602	A	19860630	198808	
US 4775880	A	19881004	US 86943705	A	19861219	198842	
KR 9007608	B	19851017				199203	
EP 228023	B1	19930602	EP 86117518	A	19861216	199322	
DE 3688520	G	19930708	DE 3688520	A	19861216	199328	
			EP 86117518	A	19861216		

Priority Applications (No Type Date): JP 86151602 A 19860630; JP 85293135 A 19851227; JP 8672981 A 19860331

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 228023	A	E	12		
Designated States (Regional): DE FR					
US 4775880	A		10		
EP 228023	B1	E	13	H01L-027/14	
Designated States (Regional): DE					
DE 3688520	G			H01L-027/14	Based on patent EP 228023

Solid-state image sensor with photoconductive cell array **- ...**

...**has signal detecting pre-** amplifier **connected to common electrodes through analog switches and load resistor**

...Abstract (Basic): detector senses image signals sequentially supplied from the photoelectric converting elements to produce an electrical **video** image signal. The signal detector is connected to the other group of the electrodes...

... **USE** /ADVANTAGE - Copier. Improved signal-to-noise ratio
...Abstract (Equivalent): detector senses image signals sequentially supplied from the photoelectric converting elements to produce an electrical **video** image signal. The signal detector is connected to the other group of the electrodes...

... **USE** /ADVANTAGE - Copier. Improved signal-to-noise ratio. (12pp Dwg.No.1/5)
...Abstract (Equivalent): cell unit the both side-ended teeth of the corresp. common electrode, so that the **adjacent** side-ended teeth of the neighbouring common electrodes are electrically shielded by the side-ended teeth of the cell electrodes. A signal detecting pre-**amplifier** is connected to the common electrodes through analogue switches and a load resistor...

... **USE** /ADVANTAGE - Reads input paper document to produce high-quality image signal at high speed. (10pp)
...Title Terms: **ARRAY** ;

29/3,K/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004715851
WPI Acc No: 1986-219193/198634
XRPX Acc No: N86-163569
Medical diagnostic X-ray picture prodn. system - has sensitive screen scanned by laser and connected to detectors by optical fibres
Patent Assignee: SIEMENS AG (SIEI)
Inventor: VIETH M
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3503711	A	19860814	DE 3503711	A	19850204	198634	B
EP 191322	A	19860820	EP 86100753	A	19860121	198634	
JP 61182368	A	19860815	JP 8620013	A	19860131	198639	
US 4703177	A	19871027	US 86820207	A	19860117	198745	
EP 191322	B	19881214				198850	
DE 3661449	G	19890119				198904	

Priority Applications (No Type Date): DE 3503711 A 19850204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3503711	A		19		
EP 191322	A	G			
Designated States (Regional): DE FR					
EP 191322	B	G			
Designated States (Regional): DE FR					

...Abstract (Basic): the intensity of the incident X-rays, line by line. A red laser may be **used** , and the plate may glow blue where it is

excited by the laser beam...

...then the next four points (A21-24) and so on. Each detector has its own **amplifier** (31-34) connected to a sample-and-hold peak recorder circuit (36-39). A multiplexer...

... **USE** /ADVANTAGE - Prodn. of **sharp** good quality X-ray pictures.
...Abstract (Equivalent): 14) for the linewise scanning of the photo-stimulated luminescence of the storage plate (10) **using** a laser (16) and for transferring the light signals with light guides (30,40), which...

...46) is associated, characterised in that several detectors (21 to 24) are provided, with which **several** respective **picture** **elements** (A11,A21,A31...An1) of a picture line (Z1) are associated in such a way ...
...Abstract (Equivalent): The X-ray camera with a storage plate is **used** to generate an image to be read by a reproducer with an image reader to ...

...photo-stimulated luminescence of the storage plate. Several detectors are provided, each being correlated with **several** **picture** **elements** of a picture line that consecutive picture elements are each connected via a light waveguide of an **array** of light waveguides to different detectors...

...Each photo-stimulated light signal of an **adjacent** picture element is processed by a different detector so that afterglow of the picture elements...

29/3,K/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003957175
WPI Acc No: 1984-102719/198417
XRPX Acc No: N84-076277
Processing and inspecting system for fruit - illuminates each item in four directions with polarised light and detects filtered reflected light to detect colour and check for blemishes
Patent Assignee: MILLS G A (MILL-I); PENNWALT CORP (PENN)
Inventor: MILLS G A
Number of Countries: 010 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 105453	A	19840418	EP 83109638	A	19830927	198417	B
ZA 8304924	A	19840210				198418	
AU 8316436	A	19840405				198421	
BR 8305174	A	19840502				198425	
ES 8405644	A	19841001				198449	
US 4534470	A	19850813	US 82430084	A	19820930	198535	
IL 68395	A	19860530				198639	
EP 105453	B	19890809				198932	

Priority Applications (No Type Date): US 82430084 A 19820930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 105453	A	E	39		

Designated States (Regional): FR GB IT NL

EP 105453 B E
Designated States (Regional): FR GB IT NL

...Abstract (Basic): separated file past an examination station (22) where the fruit (10) is rotated under a **video** system or optical scanning unit. Each **video** system includes an illuminated subsystem and a detector subsystem. Four light sources illuminate the fruit...

...The polarizer (P1), lens (L1) and filter (F1) together with diodes (DO and D11) and **amplifier** multiplexor (62,64) scan the whole surface of the fruit as it rotates to detect...
...Abstract (Equivalent): signal means (18) comprising: means (20) for illuminating each said itme (10); at least one **array** (61) of light detectors (D0 to D11), said **array** (61) being positoined so that each said detector (D0 to D11) generates a signal representative...

...for obtaining a plurality of comparision signals representing comparison of data signals corresponding to respective **adjacent** portions (PB0 to PB11) of the...

...moving it underneath said illuminating means (20) while said item is being rotated: (c) said **array** (619 being further positioned such that said portions (PB0 to PB11) of the surface of...
...Abstract (Equivalent): number of difference signals are obtained by subtracting the values of data signals corresponding to **adjacent** portions of the surface of each item, and **used** for sorting the items ...

29/3,K/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003381256
WPI Acc No: 1982-N9291E/198242
Colour shadow mask cathode ray tube - has arrays **of three phosphors radiating three colours such that third colour is produced when the other two colours are combined**
Patent Assignee: HAINES D (HAIN-I); TEKTRONIX INC (TEKT)
Inventor: KAUFMAN M; TAYLOR K
Number of Countries: 004 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8203494	A	19821014				198242	B
DE 3239730	A	19830324	DE 239730	A	19820325	198313	
EP 75592	A	19830406				198315	
GB 2108315	A	19830511	GB 8233552	A	19820330	198319	
GB 2108315	B	19841024				198443	
US 4488093	A	19841211	US 82456932	A	19821001	198501	
DE 3239730	C	19880211				198806	

Priority Applications (No Type Date): JP 8148312 A 19810331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8203494	A	E	17		

Designated States (National): DE GB US
Designated States (Regional): FR
EP 75592 A E
Designated States (Regional): FR

... **has** arrays **of three phosphors radiating three colours such that third colour is produced when the other...**

...Abstract (Basic): The phosphor **arrays** are deposited on the back of the faceplate, of the tube, in a black matrix...

...which sense logic signals for a product being tested. A control unit (14) controls four **video** parameters characterising the display mode, which are; character colour, field colour, intermittent display and reverse **video** mode...

...Three electron guns (42,44,46) are driven by respective Z-axis **amplifiers** (36,38,40) so as to provide three electron beams of which scanning is caused by a deflection circuit (34) and deflection coils (48). A ROM (26) determines the **video** parameters of each character displayed. By **using** yellow as the third colour, an area of yellow can be produced within, or **adjacent** to, a larger area of red by irradiating both the red and green phosphors within...

...Title Terms: **ARRAY** ;

?

31/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011385996 **Image available**
WPI Acc No: 1997-363903/199733
XRPX Acc No: N97-302499

CMOS imaging device with integrated **flash** memory **image correction circuitry - comprising sensor array and flash programmable** memory **array on single** integrated **circuit,** memory **array storing compensation values for adjusting signals output from sensor array**

Patent Assignee: INTEL CORP (ITLC)
Inventor: HIRT R; ROLLENDER M
Number of Countries: 075 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9724728	A1	19970710	WO 96US20870	A	19961227	199733	B
AU 9716898	A	19970728	AU 9716898	A	19961227	199746	
US 5883830	A	19990316	US 95581403	A	19951229	199918	
			US 97855658	A	19970513		
TW 399340	A	20000721	TW 97101069	A	19970130	200111	

Priority Applications (No Type Date): US 95581403 A 19951229; US 97855658 A 19970513

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9724728	A1	E	23	G11C-007/00	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN

Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG

Patent No	Kind	Main IPC	Filing Notes
AU 9716898	A	G11C-007/00	Based on patent WO 9724728
US 5883830	A	G11C-011/34	Cont of application US 95581403
TW 399340	A	H01L-031/00	

CMOS imaging device with integrated **flash** memory **image correction circuitry...**

...**comprising sensor array and flash programmable** memory **array on single** integrated **circuit,** memory **array storing compensation values for adjusting signals output from sensor array**

...Abstract (Basic): integrated circuit includes a sensor array (12) and compensation circuitry (14). The sensor array has **several** individual **pixel** sensor elements which produce signals indicative of the incident light. The compensation circuitry adjusts signals...

...process variations. A flash programmable memory array stores compensation values for adjusting the signals. A **controller** **circuit** adjusts the signals from the sensor array...

31/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009073894 **Image available**
WPI Acc No: 1992-201313/199225

XRPX Acc No: N92-152358

Control unit for flat e.g. liquid crystal display panel - has reference table with data for control of colour information

Patent Assignee: HITACHI LTD (HITA); HITACHI VIDEO & INFORMATION SYST (HITA-N)

Inventor: JINUSHI M; NISHIOKA K; TSUCHIYA N; TSUCHIYA M

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4139704	A	19920611	DE 4139704	A	19911202	199225	B
US 5329292	A	19940712	US 91796678	A	19911125	199427	
US 5539431	A	19960723	US 91796678	A	19911125	199635	
			US 94224177	A	19940407		
KR 9503981	B1	19950421	KR 9121598	A	19911128	199710	N
US 5652605	A	19970729	US 91796678	A	19911125	199736	
			US 94224177	A	19940407		
			US 95564869	A	19951130		

Priority Applications (No Type Date): JP 90328891 A 19901130; KR 9121598 A 19911128

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4139704	A		24		
US 5329292	A		23		
US 5539431	A		23		Div ex application US 91796678
					Div ex patent US 5329292
US 5652605	A		17		Div ex application US 91796678
					Div ex application US 94224177
					Div ex patent US 5329292

...Abstract (Basic): The display panel providing a multicolour facility is operated by a **controller** with a timing **circuit** (3a) receiving an input from an oscillator (1a). The system has a display address generator...

...Abstract (Equivalent): to a display device, a display interface circuit for outputting image data composed of a **plurality** of **pixels** read out of said parallel lookup table in synchronous with an input timing of said display device, and a flat panel display for displaying said image data composed of said **plurality** of **pixels** read out of said display interface circuit, wherein said parallel lookup table **includes** **memory** means of n in number (where n is an integer greater than one) for storing...

...a flat display device which displays an image made up of a **plurality** of **pixels** from the data provided by said parallel look up table...

?

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File 348:EUROPEAN PATENTS 1978-2004/Mar W03
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040325,UT=20040318
         (c) 2004 WIPO/Univentio

Set     Items   Description
S1         26   SENSE(3N)AMPLIFIER?(5N)(SHARED OR USED)(3N)(ADJACENT? OR A-
             DJOIN?)(3N)ARRAY?
S2       2988    (INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN?)(3N)MEMORY(7N)CO-
             NTROLLER(3N)(IC OR INTEGRATED()CIRCUIT? OR CHIP?? OR CIRCUIT?-
             ?)
S3          0    (STORE OR STRONG OR STORED OR STORES OR PLACE OR PLACEMENT
             OR PLACING)(3N)(ROW?? OR LINE?)(3N)(NONADJOIN? OR NONADJACENT?
              OR NON-ADJACEN?)(3N)ARRAY?
S4     112160   VIDEO
S5      13026    (PLURAL? OR MANY OR SEVERAL OR NUMEROUS OR MANY OR MULTI OR
              MULTIPLE)(3N)(PIXEL? OR PEL OR PICTURE()ELEMENT? OR PICTURE(-
             3N)CELL??)
S6      19086   HORIZONTAL(3N)LINE?
S7      40578   IMAGE(3N)DISPLAY?
S8      56601    (FIRST OR SECOND OR TWO OR 2 TOP OR BOTTOM)(3N)(HALF OR HA-
             LVES)
S9        469    (EVEN OR ODD)(3N)NUMBER?(3N)ARRAY?
S10      6943   FRAME(3N)BUFFER?
S11        42   PROCESSOR?(5N)(TRACK? OR MONITOR? OR DETECT? OR DETERMIN?)-
             (7N)(ACTIVE OR OPEN OR OFF)(5N)ARRAY??
S12    131947   IC=(G11C? OR G06F?)
S13         0   S1(S)S2(S)S5
S14         0   S1(S)S2
S15         0   S1(S)S5
S16         0   S1(S)S4
S17         2   S1(S)S5:S11
S18         2   IDPAT (sorted in duplicate/non-duplicate order)
S19         2   IDPAT (primary/non-duplicate records only)
S20         0   S5(S)S11
S21         0   S4(S)S1
S22       284   S4(S)S2
S23         3   S22(S)S5
S24         3   S23 NOT S17
S25         2   S22(S)S8
S26         1   S25 NOT (S23 OR S17)
S27         1   S22(S)S9
S28         1   S27 NOT (S25 OR S23 OR S17)
S29        34   S22(S)S10
S30         0   S29(S)S11
S31        22   S29 AND S12
S32         0   S31 AND AD=19960809:19991231/PR
S33         5   S31 AND AD=20000101:20040329/PR
S34        17   S31 NOT S33
S35        17   S34 NOT (S27 OR S25 OR S23 OR S17)
S36        17   IDPAT (sorted in duplicate/non-duplicate order)
S37        17   IDPAT (primary/non-duplicate records only)
```

19/3,K/1   (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01624456
MRAM architecture
MRAM Architektur
MRAM architecture
PATENT ASSIGNEE:
  Hewlett-Packard Company, (206037), 3000 Hanover Street, Palo Alto, CA
    94304, (US), (Applicant designated States: all)
INVENTOR:
  Lee, Heon, 455 Brahms Way 230, Sunnyvale, CA 94087, (US)
  Perder, Frederick A., 3234 Ramona Street, Palo Alto, CA 94306, (US)
LEGAL REPRESENTATIVE:
  Jehan, Robert et al (72665), Williams Powell, Morley House, 26-30 Holborn
    Viaduct, London EC1A 2BP, (GB)
PATENT (CC, No, Kind, Date): EP 1339067 A1 030827 (Basic)
APPLICATION (CC, No, Date):   EP 2003250993 030218;
PRIORITY (CC, No, Date): US 79311 020220
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR;
  HU; IE; IT; LI; LU; MC; NL; PT; SE; SI; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO
INTERNATIONAL PATENT CLASS: G11C-011/16; G11C-011/15
ABSTRACT WORD COUNT: 282
NOTE:
  Figure number on first page: 3

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200335	365
SPEC A	(English)	200335	4454
Total word count - document A			4819
Total word count - document B			0
Total word count - documents A + B			4819

...SPECIFICATION path, increasing the sneak path resistance. Increased sneak path resistance improves the signal from the **sense amplifier** and reduces the sensor noise and the net is improved **sense amplifier** performance.

The common global word lines are **shared** between two separate, but **adjacent arrays** of MRAM memory cells. Therefore, only five conductive layers are required per two arrays of...

...a less efficient structure because three conductive layers are required for each array, versus the **two** and a **half** conductor layers required for each array in the described embodiments.

Figure 4 shows another embodiment...

19/3,K/2   (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00684632
Dynamic memory having a ground control circuit
Dynamischer Speicher mit einer Massensteuerschaltung
Memoire dynamique avec un circuit de commande de masse
PATENT ASSIGNEE:

NEC CORPORATION, (236690), 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP),
(Proprietor designated states: all)

INVENTOR:
Koike, Hiroki, c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP)

LEGAL REPRESENTATIVE:
Glawe, Delfs, Moll & Partner (100692), Patentanwalte Postfach 26 01 62, 80058 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 654789 A2 950524 (Basic)
EP 654789 A3 950830
EP 654789 B1 000126

APPLICATION (CC, No, Date): EP 94118227 941118;
PRIORITY (CC, No, Date): JP 93288930 931118
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G11C-011/409; G11C-007/00
ABSTRACT WORD COUNT: 200
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200004	719
CLAIMS B	(German)	200004	675
CLAIMS B	(French)	200004	848
SPEC B	(English)	200004	3198
Total word count - document A			0
Total word count - document B			5440
Total word count - documents A + B			5440

?

24/3,K/1   (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00985206   **Image available**
IMAGE SENSING APPARATUS INCLUDING A MICROCONTROLLER
APPAREIL DE DETECTION D'IMAGE COMPRENANT UN MICROCONTROLEUR
Patent Applicant/Assignee:
  SILVERBROOK RESEARCH PTY LTD, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  SILVERBROOK Kia, Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (Designated only for: US)
Legal Representative:
  SILVERBROOK Kia (agent), Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200315395 A1 20030220 (WO 0315395)
  Application: WO 2002AU919 20020709 (PCT/WO AU0200919)
  Priority Application: US 2001922274 20010806
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
  CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
  KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
  RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
  (EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 142364

Fulltext Availability:
  Detailed Description

Detailed Description
... controller is provided that issues a long instruction word every cycle. Each instruction consists of **multiple** independent parallel operations. Further, each operation requires a statically known number of cycles to complete...using microcontrollers to achieve low cost, yet complex image processing devices.

A microcontroller is an **integrated** **chip** that **includes** , on one **chip** , all or most of the components needed for a **controller** . A microcontroller is what is known as a "system on a **chip** ." A microcontrollcr can typically **include** the following components.

CPU (central processing unit);
RAM (Random Access Memory);
EPRONYPROM/ROM (Erasable Programmable...the invention, including an APS; Fig IF includes a schematic block diagram of a digital **video** camera of the invention; Fig. 2 is a schematic block diagram of the main Artcam... In Fig. IF, reference numeral 32a generally indicates a schematic block diagram of a digital **video** camera, in accordance with the invention. With reference to Figs. ID and IE, like

24/3,K/2   (Item 2 from file: 349)

00811803 **Image available**
VIDEO, AUDIO AND GRAPHICS DECODE, COMPOSITE AND DISPLAY SYSTEM
SYSTEME COMPOSITE DE PRESENTATION A DECODAGE VIDEO AUDIO ET GRAPHIQUE

Patent Applicant/Assignee:
BROADCOM CORPORATION, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
MACINNIS Alexander G, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
TANG Chengfuh Jeffrey, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
XIE Xiaodong, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), CN (Nationality), (Designated only for: US)
KRANAWETTER Greg A, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
HSIUN Vivian, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
CHEUNG Francis, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
BHATIA Sandeep, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), IN (Nationality), (Designated only for: US)
VALMIKI Ramanujan, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), IN (Nationality), (Designated only for: US)
KUMAR Sathish, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
JEON Jun-Young E (agent), Christie, Parker & Hale LLP, Post Office Box 7068, Pasadena, CA 91109-7068, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200145426 A1 20010621 (WO 0145426)
Application: WO 2000US33757 20001213 (PCT/WO US0033757)
Priority Application: US 99170866 19991214; US 2000641374 20000818; US 2000641936 20000818; US 2000643223 20000818; US 2000640870 20000818; US 2000640869 20000818; US 2000641930 20000818; US 2000641935 20000818; US 2000642510 20000818; US 2000642458 20000818
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
((OAPI utility model)) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 85836

Fulltext Availability:
Detailed Description

Detailed Description
... are 8 possible first pixels in the first word. Using this field, 0 to 7 **pixels** may be skipped, making the Ist to the 8 th pixel in the word appear...window
controller to the display engine. All of the required control information from the window **controller** preferably is conveyed to the display engine such that all of the re.levant variables from the window **controller** are properly controlled in a timely fashion

and such that the control is not dependent...V and alpha components occupying eight
bits. The conversion process is generally dependent on the **pixel** format type and the alpha specification method, both of which are indicated by the window...in the clock selection vector may vary accordingly. Clock switching logic preferably switches between the **memory** clock and the display clock in accordance with the clock selection vector. The clock selection vector is preferably also used to multiplex the **memory** clock buffer control signals and the display clock buffer control signals.

Since there is preferably...start address since any blanking at the start will simply have
an effect of shifting **pixels** to the left. Further, the shifting to the right cannot be achieved by blanking some...function of all pixels of all graphical elements for every frame or field of the **video** in a timely manner.

The system preferably displays a graphical element by filtering the graphical...

24/3,K/3 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00253670 **Image available**
A SINGLE CHIP INTEGRATED CIRCUIT SYSTEM ARCHITECTURE FOR VIDEO-INSTRUCTION-SET-COMPUTING
ARCHITECTURE DE CIRCUIT INTEGRE MONOPUCE POUR LE CALCUL PAR JEUX D'INSTRUCTIONS VIDEO
Patent Applicant/Assignee:
SHAW Venson M,
SHAW Steven M,
Inventor(s):
SHAW Venson M,
SHAW Steven M,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9401824 A1 19940120
Application: WO 93US5863 19930617 (PCT/WO US9305863)
Priority Application: US 92909312 19920706
Designated States: AT AU BB BG BR CA CH DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO PL RO RU SD SE US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 24238
Fulltext Availability:
Claims

Claim
... for universal video encoding and decoding
including programmable signal processor for selective execution of a **plurality** **pixel** domain or frequency domain coding algorithms,, said means comprises programmable encoding circuit for receiving -input macrblocks and generating selective JPEG,, MPEGI H*2610, VQf or alike encoded **video** tokens in accordance with application input requirement, said means also comprise programmable decoding circuit for...

...scalable formatting comprises programmable

26/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00156314
SIGNAL PROCESSING APPARATUS AND METHODS
DISPOSITIF ET PROCEDES DE TRAITEMENT DE SIGNAUX
Patent Applicant/Assignee:
HARVEY John C,
Inventor(s):
HARVEY John C,
CUDDIHY James W,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8902682 A1 19890323
Application: WO 88US3000 19880908 (PCT/WO US8803000)
Priority Application: US 8796 19870911
Designated States: AT AU BE BJ BR CF CG CH CM DE DK FI FR GA GB GB HU IT JP KP LK LU MC MG ML MR MW NL NO RO SE SN SU TD TG
Publication Language: English
Fulltext Word Count: 161690
?

28/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01048015 **Image available**
HUB ARRAY SYSTEM AND METHOD
SYSTEME ET PROCEDE DE GROUPEMENT DE CONCENTRATEURS
Patent Applicant/Assignee:
  AXIS SYSTEMS INC, 209 Java Drive, Sunnyvale, CA 94089, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  LIN Sharon Sheau-Pyng, 10122 Berkshire Court, Cupertino, CA 95014, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
  BENZ William H (agent), Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313-1404, US,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200377078 A2-A3 20030918 (WO 0377078)
  Application: WO 2003US7313 20030306 (PCT/WO US0307313)
  Priority Application: US 200292839 20020306
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PH PL PT RO RU SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
  (EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 121263

Fulltext Availability:
  Detailed Description

Detailed Description
... IMPLEMENTATION SCHEMES
  A. OVERVIEW
  B. ADDRESS POINTER
  C. GATED DATA/CLOCK NETWORK ANALYSIS
  D. FPGA **ARRAY** AND CONTROL
  E. ALTERNATE EMBODIMENT USING DENSER FPGA CHIPS
  F. TIGF LOGIC DEVICES
  G. DYNAMIC...thin-film fuses therebetween. The Vcc-HI is provided to the CONFIG# to all FPGA **chips** and LINTI# to a LOCAL-BUS 708.
  The CTRL-FPGA unit 701 is the primary **controller** for FPGA 1/0 **controller** 700 to handle the various control, test, and read/write substantive data among the various...power and ground.

  FIG. 37 shows the FPGA interconnect pin-outs for a single FPGA **chip** in accordance with one embodiment of the present invention. Each **chip** 1510 may
?

37/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00989819
A single chip controller-memory device and a memory architecture and methods suitable for implementing the same
Einchipsteuerungsspeicheranordnung und eine Speicherarchitektur und Verfahren zur Inbetriebnahme derselben
Dispositif a memoire/controleur monopuce, et architecture de memoire et procede destines a mettre en oeuvre ce dispositif
PATENT ASSIGNEE:
CIRRUS LOGIC, INC., (1079714), 3100 West Warren Avenue, BS-906, Fremont, CA 94538-6423, (US), (Proprietor designated states: all)
INVENTOR:
Rao, G.R.Mohan, 1404 Westmont Drive, McKinney, Texas 75070, (US)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. High Holborn 2-5 Warwick Court, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 895246 A1 990203 (Basic)
EP 895246 B1 011121
APPLICATION (CC, No, Date): EP 98202230 950508;
PRIORITY (CC, No, Date): US 239608 940509
DESIGNATED STATES: BE; DE; ES; FR; GB; IE; IT; NL; PT
RELATED PARENT NUMBER(S) - PN (AN):
EP 760155 (EP 95919078)
INTERNATIONAL PATENT CLASS: **G11C-011/00** ; **G11C-007/00** ; **G06F-011/00**
ABSTRACT WORD COUNT: 103
NOTE:
Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199905	1164
CLAIMS B	(English)	200147	168
CLAIMS B	(German)	200147	160
CLAIMS B	(French)	200147	197
SPEC A	(English)	199905	4521
SPEC B	(English)	200147	3837
Total word count - document A			5686
Total word count - document B			4362
Total word count - documents A + B			10048

INTERNATIONAL PATENT CLASS: **G11C-011/00** ...

... **G11C-007/00** ...
... **G06F-011/00**

...SPECIFICATION B1
The present invention relates in general to digital electronic **circuits** and systems and in particular to a single **chip** **controller** - **memory** device and a **memory** architecture suitable for implementing the same.
A typical processing system with **video** /graphics display capability **includes** a central processing unit (CPU), a display controller coupled with the CPU by a system bus, a system memory also coupled to the system bus, a **frame** **buffer** coupled to the display controller by a local bus, peripheral circuitry (e.g., clock drivers...

...be displayed on the display unit. The display controller, which may for example be a **video** graphics architecture (VGA) controller, generally interfaces the CPU and the display driver circuitry, exchanges graphics and/or **video** data with the **frame buffer** during data processing and display refresh operations, controls **frame buffer** memory operations, and performs additional processing on the subject graphics or **video** data, such as color expansion. The display driver circuitry converts digital data received from the display controller into the analog levels required by the display unit to generate graphics/ **video** display images. The display unit may be any type of device which presents images to the user conveying the information represented by the graphics/ **video** data being processed. The "display" may also be a printer or other document view/print...

37/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00885900
Hot-plugging circuit for connecting peripherals to a computer
Einsteckschaltung unter Spannung zum Anschluss von Peripheriegeraten an einen Rechner
Circuit pour la connexion enfichable sous tension de dispositifs peripheriques a un ordinateur
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Boesch, Shannon C., 205 Parque Vista Drive, Georgetown, Texas 78626, (US)
Haley, Charles L., 3505 Antelope Trail, Temple, Texas 76504, (US)
LEGAL REPRESENTATIVE:
Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, Northumberland House, 303-306 High Holborn, London WC1V 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 810531 A1 971203 (Basic)
APPLICATION (CC, No, Date): EP 97303496 970522;
PRIORITY (CC, No, Date): US 656799 960531
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-013/40**
ABSTRACT WORD COUNT: 100

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9711W4	402
SPEC A	(English)	9711W4	3623
Total word count - document A			4025
Total word count - document B			0
Total word count - documents A + B			4025

INTERNATIONAL PATENT CLASS: **G06F-013/40**

...SPECIFICATION 12.
Figure 2 illustrates a block diagram of the computer system 10. The system processing **circuitry** 22 **includes** , in part, a central processing unit (CPU) 24, a system BIOS 26, main **memory** 28, floppy **controller** 29, **video** /graphics **controller** 30, **frame buffer** 32 and modem 33 (**including** asynchronous I/O **circuitry**). The system processing circuitry 22 communicates with the keyboard 18 and the display 20. In...

37/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00805683
Texel cache interrupt daemon for virtual memory management of texture maps
Programmunterbrechung durch einen Pufferspeicher um Texturabbildungsdaten in einem virtuellen Speicher zu verwalten
Programme d'interruption par un cache pour allouer de l'espace de memoire virtuelle a des tables de topographie de texture
PATENT ASSIGNEE:
Hewlett-Packard Company, (206030), 3000 Hanover Street, Palo Alto, California 94304, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Gannet, Ethan W., 2607 Shadow Mountain Drive, Ft. Collins, CO 80525, (US)
LEGAL REPRESENTATIVE:
Schoppe, Fritz, Dipl.-Ing. (55463), Patentanwalt, Georg-Kalb-Strasse 9, 82049 Pullach, (DE)
PATENT (CC, No, Kind, Date): EP 749100 A2 961218 (Basic)
EP 749100 A3 990526
APPLICATION (CC, No, Date): EP 96107382 960509;
PRIORITY (CC, No, Date): US 486447 950608
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06T-015/10; **G06F-012/12** ; **G06F-012/08**
ABSTRACT WORD COUNT: 198

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	937
SPEC A	(English)	EPAB96	44761
Total word count - document A			45698
Total word count - document B			0
Total word count - documents A + B			45698

...INTERNATIONAL PATENT CLASS: **G06F-012/12** ...

... **G06F-012/08**

...SPECIFICATION texture data for each pixel is provided by the texture mapping chip 46 to the **frame buffer** board over five buses 28. The five buses 28 are respectively coupled to five **frame buffer** controller chips 50A, 50B, 50C, 50D and 50E provided on the **frame buffer** board, and provide resultant texture data to the **frame buffer** controller **chips** in parallel. The frame **buffer controller chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) chips 51A-E. The **frame buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame buffer controller chips** control different, non-overlapping segments of the display screen. Each **frame buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame buffer** controller chips interpolate the primitive data to compute the screen display pixel coordinates in their...

...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame buffer** controller chips combine, on

a pixel by pixel basis, the object color values and the...

37/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00803648
Cache system with simultaneous tag comparison
Cache-Speicheranordnung mit gleichzeitigem Etikettenvergleich
Systeme d'antememoire a comparaison simultanee d'etiquettes
PATENT ASSIGNEE:
Hewlett-Packard Company, A Delaware Corporation, (3016020), 3000 Hanover Street, Palo Alto, CA 94304, (US), (Proprietor designated states: all)
INVENTOR:
Emmot, Darel N., 3931 Moss Creek Drive, Fort Collins, CO 80526, (US)
LEGAL REPRESENTATIVE:
Schoppe, Fritz, Dipl.-Ing. (55463), Schoppe, Zimmermann & Stockeler Patentanwalte Postfach 71 08 67, 81458 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 747826 A2 961211 (Basic)
EP 747826 A3 980401
EP 747826 B1 010919
APPLICATION (CC, No, Date): EP 96107605 960513;
PRIORITY (CC, No, Date): US 471653 950606
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-012/08** ; **G06F-012/10**
ABSTRACT WORD COUNT: 206
NOTE:
Figure number on first page: 24

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1376
CLAIMS B	(English)	200138	1180
CLAIMS B	(German)	200138	1018
CLAIMS B	(French)	200138	1204
SPEC A	(English)	EPAB96	30735
SPEC B	(English)	200138	30375
Total word count - document A			32117
Total word count - document B			33777
Total word count - documents A + B			65894

INTERNATIONAL PATENT CLASS: **G06F-012/08** ...

... **G06F-012/10**

...SPECIFICATION on the frame buffer board, and provide resultant texture data to the frame buffer controller **chips** in parallel. The frame **buffer controller chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) **chips** 51A-E. The **frame buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame buffer controller chips** control different, non-overlapping segments of the display screen. Each **frame buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame buffer** controller chips interpolate the primitive data to compute the screen display pixel coordinates in their...

...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame buffer** controller chips combine, on a pixel by pixel basis, the object color values and the...

...SPECIFICATION and provide output primitive data over bus 18 to the texture mapping chip and the **frame buffer** board, while the texture data associated with a primitive that caused the cache miss is...

...texture data for each pixel is provided by the texture mapping chip 46 to the **frame buffer** board over five buses 28. The five buses 28 are respectively coupled to five **frame buffer** controller chips 50A, 50B, 50C, 50D and 50E provided on the **frame buffer** board, and provide resultant texture data to the **frame buffer** controller **chips** in parallel. The frame **buffer controller chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) **chips** 51A-E. The **frame buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame buffer controller chips** control different, non-overlapping segments of the display screen. Each **frame buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame buffer** controller chips interpolate the primitive data to compute the screen display pixel coordinates in their...

...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame buffer** controller chips combine, on a pixel by pixel basis, the object color values and the...

37/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00803637
Interrupt scheme for updating a local memory
Unterbrechungsschema zum Aktualisieren eines Lokalspeichers
Schema d'interruption pour actualiser une memoire locale
PATENT ASSIGNEE:
  Hewlett-Packard Company, (206030), 3000 Hanover Street, Palo Alto, California 94304, (US), (Applicant designated States: all)
INVENTOR:
  Alcorn, Byron A., 3931 Benthaven Street, Fort Collins, CO 80526, (US)
  Emmot, Darel N., 3931 Moss Creek Drive, Fort Collins, CO 80526, (US)
  Tucker, Steven Paul, 817 Prescott Street, Fort Collins, CO 80526, (US)
LEGAL REPRESENTATIVE:
  Schoppe, Fritz, Dipl.-Ing. (55463), Schoppe & Zimmermann Patentanwalte Postfach 71 08 67, 81458 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 747859 A2 961211 (Basic)
                             EP 747859 A3 990901
APPLICATION (CC, No, Date): EP 96107381 960509;
PRIORITY (CC, No, Date): US 469057 950606
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06T-015/10; **G06F-012/12** ; **G06F-012/08**
ABSTRACT WORD COUNT: 204
NOTE:
  Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

```
Available Text  Language   Update    Word Count
      CLAIMS A  (English)  EPAB96     1306
      SPEC A    (English)  EPAB96    30756
Total word count - document A        32062
Total word count - document B            0
Total word count - documents A + B   32062
```

...INTERNATIONAL PATENT CLASS: **G06F-012/12** ...

... **G06F-012/08**

...SPECIFICATION and provide output primitive data over bus 18 to the texture mapping chip and the **frame** **buffer** board, while the texture data associated with a primitive that caused the cache miss is...

...texture data for each pixel is provided by the texture mapping chip 46 to the **frame** **buffer** board over five buses 28. The five buses 28 are respectively coupled to five **frame** **buffer** controller chips 50A, 50B, 50C, 50D and 50E provided on the **frame** **buffer** board, and provide resultant texture data to the **frame** **buffer** controller **chips** in parallel. The frame **buffer** **controller** **chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) **chips** 51A-E. The **frame** **buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame** **buffer** **controller** **chips** control different, non-overlapping segments of the display screen. Each **frame** **buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame** **buffer** controller chips interpolate the primitive data to compute the screen display pixel coordinates in their...

...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame** **buffer** controller chips combine, on a pixel by pixel basis, the object color values and the...

37/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00803627
SDRAM data allocation system and method
SDRAM-Datenzuweisungsanordnung und -verfahren
Systeme et procede d'affectation de donnees de SDRAM
PATENT ASSIGNEE:
  Hewlett-Packard Company, A Delaware Corporation, (3016020), 3000 Hanover Street, Palo Alto, CA 94304, (US), (Proprietor designated states: all)
INVENTOR:
  Dykstal, John, 4028 Platte Drive, Fort Collins, CO 80526, (US)
  Alcorn, Byron A., 3931 Benthaven Street, Fort Collins, CO 80526, (US)
  Emmot, Darel N., 3931 Moss Creek Drive, Fort Collins, CO 80526, (US)
LEGAL REPRESENTATIVE:
  Schoppe, Fritz, Dipl.-Ing. (55463), Schoppe, Zimmermann & Stockeler Patentanwalte Postfach 71 08 67, 81458 Munchen, (DE)

```
PATENT (CC, No, Kind, Date):  EP 747825  A2  961211 (Basic)
                              EP 747825  A3  980318
                              EP 747825  B1  010919
APPLICATION (CC, No, Date):   EP 96107221 960507;
PRIORITY (CC, No, Date): US 466865 950606
```

DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-012/06** ; **G06F-012/08**
ABSTRACT WORD COUNT: 143
NOTE:
Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	535
CLAIMS B	(English)	200138	693
CLAIMS B	(German)	200138	705
CLAIMS B	(French)	200138	760
SPEC A	(English)	EPAB96	30684
SPEC B	(English)	200138	30296
Total word count - document A			31224
Total word count - document B			32454
Total word count - documents A + B			63678

INTERNATIONAL PATENT CLASS: **G06F-012/06** ...

... **G06F-012/08**

...SPECIFICATION on the frame buffer board, and provide resultant texture data to the frame buffer controller **chips** in parallel. The frame **buffer controller chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) **chips** 51A-E. The **frame buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame buffer controller chips** control different, non-overlapping segments of the display screen. Each **frame buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame buffer** controller chips interpolate the primitive data to compute the screen display pixel coordinates in their...

...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame buffer** controller chips combine, on a pixel by pixel basis, the object color values and the...

...SPECIFICATION and provide output primitive data over bus 18 to the texture mapping chip and the **frame buffer** board, while the texture data associated with a primitive that caused the cache miss is...

...texture data for each pixel is provided by the texture mapping chip 46 to the **frame buffer** board over five buses 28. The five buses 28 are respectively coupled to five **frame buffer** controller chips 50A, 50B, 50C, 50D and 50E provided on the **frame buffer** board, and provide resultant texture data to the **frame buffer** controller **chips** in parallel. The frame **buffer controller chips** 50A-E are respectively coupled to groups of associated VRAM (**video** random access **memory**) **chips** 51A-E. The **frame buffer** board further **includes** four **video** format **chips** , 52A, 52B, 52C and 52D, and a RAMDAC (random access **memory** digital-to-analog converter) 54. The **frame buffer controller chips** control different, non-overlapping segments of the display screen. Each **frame buffer** controller chip receives primitive data from the front end board over bus 18, and resultant texture mapping data from the texture mapping board over bus 28. The **frame buffer** controller chips interpolate the primitive data to compute the screen

display pixel coordinates in their...
...e., triangles) for which resultant texture data is provided from the texture mapping board, the **frame** **buffer** controller chips combine, on a pixel by pixel basis, the object color values and the...

37/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00691462
Three input arithmetic logic unit forming the sum of a first and a second boolean combination of the inputs
Arithmetisch-logische Einheit mit drei Eingangen, die die Summe einer ersten und einer zweiten booleschen Kombination berechnet
Unite arithmetique et logique a trois entrees calculant la somme d'un premier et une seconde combinaison booleenne des entrees
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (Proprietor designated states: all)
INVENTOR:
Guttag, Karl M., 4015 South Sandy Court, Missouri City, Texas 77459, (US)
Simpson, Richard, 21 The Marsh, Carlton, Bedford, MK43 7JU, (GB)
Walsh, Brendan, 14, Chillingham Green, Bedford, MK41 8HT, (GB)
LEGAL REPRESENTATIVE:
Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, 20 Red Lion Street , London WC1R 4PQ, (GB)
PATENT (CC, No, Kind, Date): EP 660227 A2 950628 (Basic)
EP 660227 A3 960124
EP 660227 B1 020502
APPLICATION (CC, No, Date): EP 94308888 941130;
PRIORITY (CC, No, Date): US 160113 931130
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-007/48**
ABSTRACT WORD COUNT: 312
NOTE:
Figure number on first page: 17

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200218	1112
CLAIMS B	(German)	200218	1029
CLAIMS B	(French)	200218	1299
SPEC B	(English)	200218	43271
Total word count - document A			0
Total word count - document B			46711
Total word count - documents A + B			46711

INTERNATIONAL PATENT CLASS: **G06F-007/48**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame** **buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

37/3,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00691461

Three input arithmetic logic unit with barrel rotator

Drei-Eingange-Arithmetik-Logik-Einheit mit Trommel-Rotationsschaltung

Unite arithmethique et logique a trois entrees avec rotateur a tambour

PATENT ASSIGNEE:

TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (Proprietor designated states: all)

INVENTOR:

Guttag, Karl M., of 3907 Oakmont Ct., Sugar Land, Texas 77479, (US)
Balmer, Keith, 6 Salcombe Close, Bedford, (US)
Gove, Robert J., 1405 Scarborough Lane, Plano, Texas 75075, (US)
Read, Christopher J., 11807 Burlingame, Houston, Texas 77099, (US)
Golston, Jeremiah E., 2930 Mesquite, Sugar Land, Texas 77479, (US)
Poland, Sydney W., 22307 Prince George, Katy, Texas 77449, (US)
Ing-Simmons, Nicholas, 47 Highfield Avenue, Alconbury, Weston, Cambridgeshire, PE17 5JS, (GB)
Moyse, Philip, 12 Neville Close, Bronham, Bedford, MK43 8JG, (US)

LEGAL REPRESENTATIVE:

Blanco White, Henry Nicholas et al (50111), ABEL & IMRAY 20 Red Lion Street, London WC1R 4PQ, (GB)

PATENT (CC, No, Kind, Date): EP 660223 A2 950628 (Basic)
EP 660223 A3 960124
EP 660223 B1 011004

APPLICATION (CC, No, Date): EP 94308881 941130;

PRIORITY (CC, No, Date): US 160299 931130; US 160573 931130; US 160298 931130

DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **G06F-005/01** ; **G06F-007/00** ; **G06F-007/38**

ABSTRACT WORD COUNT: 351

NOTE:

Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200140	565
CLAIMS B	(German)	200140	475
CLAIMS B	(French)	200140	680
SPEC B	(English)	200140	44094
Total word count - document A			0
Total word count - document B			45814
Total word count - documents A + B			45814

INTERNATIONAL PATENT CLASS: **G06F-005/01** ...

... **G06F-007/00** ...

... **G06F-007/38**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

37/3,K/9 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00688594

Rotation register for orthogonal data transformation

Rotationsregister zur orthogonalen Datentransformation

Registre a rotation pour la transformation orthogonale des donnees

PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (Proprietor designated states: all)

INVENTOR:
Balmer, Keith, 6 Salcome Close, Bedford, MK40 3ba, (GB)

LEGAL REPRESENTATIVE:
Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, 20 Red Lion Street , London WC1R 4PQ, (GB)

PATENT (CC, No, Kind, Date): EP 657802 A2 950614 (Basic)
EP 657802 A3 960515
EP 657802 B1 030514

APPLICATION (CC, No, Date): EP 94308902 941130;

PRIORITY (CC, No, Date): US 159346 931130

DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **G06F-005/01** ; **G06F-009/315** ; **G11C-019/00** ; G06T-003/60

ABSTRACT WORD COUNT: 346

NOTE:
Figure number on first page: 8

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2053
CLAIMS B	(English)	200320	1797
CLAIMS B	(German)	200320	1469
CLAIMS B	(French)	200320	2262
SPEC A	(English)	EPAB95	44586
SPEC B	(English)	200320	43297
Total word count - document A			46648
Total word count - document B			48825
Total word count - documents A + B			95473

INTERNATIONAL PATENT CLASS: **G06F-005/01** ...

... **G06F-009/315** ...

... **G11C-019/00**
...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.
Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.
Multiprocessor integrated circuit 100...

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.
Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.
Multiprocessor integrated circuit 100...

37/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00688593
Three input arithmetic logic unit
Arithmetik-Logikschaltung mit drei Eingangen
Unite arithmetique logique a trois entrees
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (Proprietor designated states: all)
INVENTOR:
Guttag, Karl M., 4015 South Sandy Court, Missouri City, Texas 77459, (US)
Simpson, Richard, 21 the Marsh, Carlton, Bedford, MK43 7JU, (GB)
Walsh, Brendan, 14, Chillingham Green, Bedford, MK41 8HT, (GB)
LEGAL REPRESENTATIVE:
Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, 20 Red Lion Street , London WC1R 4PQ, (GB)
PATENT (CC, No, Kind, Date): EP 657803 A2 950614 (Basic)
EP 657803 A3 960124
EP 657803 B1 020502
APPLICATION (CC, No, Date): EP 94308901 941130;

PRIORITY (CC, No, Date): US 159345 931130
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-007/38** ; **G06F-007/48**
ABSTRACT WORD COUNT: 312
NOTE:
Figure number on first page: 10

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	1201
CLAIMS B	(English)	200218	494
CLAIMS B	(German)	200218	497
CLAIMS B	(French)	200218	557
SPEC A	(English)	EPAB95	44582
SPEC B	(English)	200218	43596
Total word count - document A			45791
Total word count - document B			45144
Total word count - documents A + B			90935

INTERNATIONAL PATENT CLASS: **G06F-007/38** ...

... **G06F-007/48**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrat**ed circuit 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

37/3,K/11 (Item 11 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00687304

Conditional memory store from a register pair
Bedingtes Speicherladen von einem Registerpaar
Chargement conditionnel de memoire d'une paire de registres

PATENT ASSIGNEE:
  TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (Proprietor designated states: all)
INVENTOR:
  Guttag, Karl M., 4015 South Sandy Court, Missouri City, Texas 77459, (US)
  Poland, Sydney W., 22307 Prince George, Katy, Texas 77449, (US)
  Balmer, Keith, 6 Salcome Close, Bedford, MK40 3BA, (GB)
LEGAL REPRESENTATIVE:
  Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, 20 Red Lion Street, London WC1R 4PQ, (GB)
PATENT (CC, No, Kind, Date): EP 656584 A1 950607 (Basic)
  EP 656584 B1 011004
APPLICATION (CC, No, Date): EP 94308832 941130;
PRIORITY (CC, No, Date): US 160118 931130
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-009/312** ; **G06F-009/318**
ABSTRACT WORD COUNT: 247
NOTE:
  Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	1542
CLAIMS B	(English)	200140	759
CLAIMS B	(German)	200140	675
CLAIMS B	(French)	200140	904
SPEC A	(English)	EPAB95	44658
SPEC B	(English)	200140	43480
Total word count - document A			46210
Total word count - document B			45818
Total word count - documents A + B			92028

INTERNATIONAL PATENT CLASS: **G06F-009/312** ...

... **G06F-009/318**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated** **circuit** 100 or external to multiprocessor **integrated** **circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated** **circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame** **buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

37/3,K/12 (Item 12 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00686235

Arithmetic and logic unit having a plurality of independent sections and a register for storing the status bits

Arithmetisch-logische Einheit mit mehreren unabhangigen Abschnitten und ein Register zur Speicherung der Statusbits

Unite arithmetique et logique ayant plusieurs sections independantes et un registre pour stocker les bits de status

PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (applicant designated states: DE;FR;GB;IT;NL)

INVENTOR:
Balmer, Keith, 6 Salcombe Close, Bedford, (GB)
Guttag, Karl M., 3907 Oakmont Ct., Sugar Land, Texas 55479, (US)
Ing-Simmons, Nicholas, 47 Highfield Avenue, Alconbury, Weston, Cambridgeshire, PE17 5JS, (GB)
Gove, Robert J., 1405 Scarborough Lane, Plano, Texas 75075, (US)
Golston, Jeremiah E., 2930 Mesquite, Sugar Land, Texas 77479, (US)
Read, Christopher J., 11807 Burlingame, Houston, Texas 77099, (US)
Poland, Sydney W., 22307 Prince George, Katy, Texas 77449, (US)

LEGAL REPRESENTATIVE:
Blanco White, Henry Nicholas et al (50111), ABEL & IMRAY 20 Red Lion Street, London WC1R 4PQ, (GB)

PATENT (CC, No, Kind, Date): EP 655680 A1 950531 (Basic)
EP 655680 B1 990728

APPLICATION (CC, No, Date): EP 94308833 941130;
PRIORITY (CC, No, Date): US 158742 931130
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-009/38** ; **G06F-009/30**
ABSTRACT WORD COUNT: 370

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9930	772
CLAIMS B	(German)	9930	745
CLAIMS B	(French)	9930	894

SPEC B (English) 9930 44572
Total word count - document A 0
Total word count - document B 46983
Total word count - documents A + B 46983

INTERNATIONAL PATENT CLASS: **G06F-009/38** ...
... **G06F-009/30**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.
Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.
Multiprocessor integrated circuit 100...

37/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00686233
Three input arithmetic logic unit forming mixed arithmetic and boolean combinations.
Arithmetisch-logische Einheit mit drei Eingangen, die gemischte arithmetische und boolesche Kombinationen macht.
Unite arithmetique et logique a trois entrees faisant des combinaisons mixtes arithmetiques et booleennes.
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Guttag, Karl M., 4015 South Sandy Court, Missouri City, Texas 77459, (US)
Simpson, Richard, 21 The Marsh, Carlton, Bedford, MK43 7JU, (GB)
Walsh, Brendan, 14, Chillingham Green, Bedford, MK41 8HT, (GB)
LEGAL REPRESENTATIVE:
Legg, Cyrus James Grahame et al (81121), ABEL & IMRAY, 20 Red Lion Street , London WC1R 4PQ, (GB)
PATENT (CC, No, Kind, Date): EP 655676 A2 950531 (Basic)
EP 655676 A3 961023
APPLICATION (CC, No, Date): EP 94308825 941130;
PRIORITY (CC, No, Date): US 159285 931130
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-007/48** ; **G06F-007/00** ; G06T-001/20; **G06F-009/30**
ABSTRACT WORD COUNT: 312

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2754

SPEC A (English) EPAB95 44578
Total word count - document A 47332
Total word count - document B 0
Total word count - documents A + B 47332

INTERNATIONAL PATENT CLASS: **G06F-007/48** ...

... **G06F-007/00** ...

... **G06F-009/30**

...SPECIFICATION information to be transferred between source and destination memory addresses, which can be within multiprocessor **integrated circuit** 100 or external to multiprocessor **integrated circuit** 100. Transfer **controller** 80 preferably also **includes** a refresh **controller** for dynamic random access **memory** (DRAM) which require periodic refresh to retain their data.

Frame **controller** 90 is the interface between multiprocessor **integrated circuit** 100 and external image capture and display systems. Frame controller 90 provides control over capture...

...by the user. These image systems would ordinarily include independent frame memories used for either **frame** grabber or **frame buffer** storage. **Frame** controlled 90 preferably operates to control **video** dynamic random access memory (VRAM) through refresh and shift register control.

Multiprocessor integrated circuit 100...

37/3,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00489888
Multimedia system
Multimediensystem
Systeme multimedia
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)
INVENTOR:
Dinwiddie, John Monroe, Jr., 112 Pacer Circle, West Palm Beach, Florida 33414, (US)
Freeman, Bobby Joe, 1381 SW 28th Avenue, Boynton Beach, Florida 33426, (US)
Suarez, Gustave Armando, 21482 Woodchuck Lane, Boca Raton, Florida 33428, (US)
Wilkie, Bruce James, 15635 Lindbergh Lane, West Palm Beach, Florida 33414 , (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 492795 A2 920701 (Basic)
EP 492795 A3 921230
EP 492795 B1 950920
EP 492795 B2 000426
APPLICATION (CC, No, Date): EP 91310692 911120;
PRIORITY (CC, No, Date): US 625564 901211
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **G06F-003/14** ; G09G-005/00

ABSTRACT WORD COUNT: 101
NOTE:
  Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200017	414
CLAIMS B	(German)	200017	408
CLAIMS B	(French)	200017	484
SPEC B	(English)	200017	12373
Total word count - document A			0
Total word count - document B			13679
Total word count - documents A + B			13679

INTERNATIONAL PATENT CLASS: **G06F-003/14** ...

...SPECIFICATION characteristics.
When functioning as an image capture facility, media control module 30 uses frame capture **circuit** 54. Frame **capture** **circuit** 54 **includes** **frame** **buffer** control **circuit** 78, **frame** **buffer** 80, which is **video** random access **memory** (VRAM), switch **circuit** 82 and **fader** **circuit** 84. Switch circuit 82 **includes** image switch 86, analog to digital (A/D) converter 88 and buffer circuit 90. Fader circuit 84 includes digital to analog converters 92, 94 and fader circuit 96. **Frame** capture **circuit** **54** receives the synchronization **signals** **PVC** SYNC, the SVC SYNC, the SYS SYNC. Frame capture circuit 54 also receives the PVC...

37/3,K/15 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00385861 **Image available**
METHOD AND STRUCTURE FOR IMPROVING DISPLAY DATA BANDWIDTH IN A UNIFIED MEMORY ARCHITECTURE SYSTEM
PROCEDE ET STRUCTURE POUR AMELIORER LA LARGEUR DE BANDE DE DONNEES D'AFFICHAGE DANS UN SYSTEME D'ARCHITECTURE DE MEMOIRE UNIFIEE
Patent Applicant/Assignee:
  MONOLOTHIC SYSTEM TECHNOLOGY INC,
Inventor(s):
  HSU Fu-Chieh,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9726604 A1 19970724
  Application: WO 97US14 19970115 (PCT/WO US9700014)
  Priority Application: US 96379 19960116
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 5331
Main International Patent Class: **G06F-015/167**
Fulltext Availability:
  Detailed Description

Detailed Description
... buffer memory

306 is the same type of memory as unified memory 304.

However, expansion **frame** **buffer** memory 306 and unified memory 304 can also be implemented using different types of memory, Because expansion **frame** **buffer** memory 306 has a relatively small capacity (i, ...less than the loading and parasitics on the unified memory data bus 314* Thus, expansion **frame** **buffer** memory 306 can be selected to operate at a higher frequency (i,e, 132 or...

...than unified memory 304, while having a narrower data bus than unified memory 304, Expansion **frame** **buffer** memory 306 can utilize multiplexed address and data signals in the manner of MDRAM (Multibank DRAM), By selecting expansion **frame** **buffer** memory 306 in this manner, the pin requirement of expansion **frame** **buffer** memory 306 is advantageously minimized. In one embodiment, expansion **frame** **buffer** memory 306 is a DRAM array which implements the multibank architecture as described in commonly...

...al., which is hereby incorporated by reference in its entirety, In a particular embodiment, expansion **frame** **buffer** memory 306 has a data bus with a width of 16-bits (2 bytes) and...

...the multibank architecture described in U,S. Patent Application Serial No, 08/270,856, expansion **frame** **buffer** memory 306 requires only 26 pins to interface with graphics controller 305, Multibank architecture is...

...system 300, the display refresh data bandwidth is divided between unified memory 304 and expansion **frame** **buffer** memory 306. In one example, one half of the display refresh data bandwidth is provided by expansion **frame** **buffer** memory 306, and the other half of the display refresh data bandwidth is provided by...

...graphics controller 305 in more detail in accordance with one embodiment of the invention. Graphics **controller** 305 **includes** display **controller** 401, graphics accelerator 402, **video** processor 403, system interface 404, unified **memory** address/control **circuit** 410, unified memory data interface 411, expansion memory address/control circuit 420, expansion memory data...

37/3,K/16 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00333027 **Image available**
CIRCUITS, SYSTEMS, AND METHODS FOR ACCOUNTING FOR DEFECTIVE CELLS IN A MEMORY DEVICE
CIRCUITS, SYSTEMES ET METHODES PERMETTANT DE DETERMINATION DES CELLULES DEFECTUEUSES DANS UNE MEMOIRE

Patent Applicant/Assignee:
  CIRRUS LOGIC INC,
Inventor(s):
  CROSS Randolph A,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9615538 A1 19960523
  Application: WO 95US14307 19951106 (PCT/WO US9514307)
  Priority Application: US 94340163 19941115
Designated States: JP KR SG AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 6533

Main International Patent Class: **G11C-029/00**
Fulltext Availability:
  Detailed Description
Detailed Description
... 104.

FIGURE 2A is a more detailed functional block diagram of display controller 103 and **frame buffer** 104 emphasizing one embodiment of the **circuitry** implementing the principles of the present invention. As shown in FIGURE 2A, display **controller** 103 **includes** graphics/ **video controller** logic **circuitry** 201, address generator 202 and an associative **memory** system 203. **Frame buffer** 104 **includes** an array of memory cells 204 arranged in M rows and N columns. The rows...to a column address received through input/output circuitry 207. Data is exchanged between graphics/ **video** controller logic circuitry 201 and memory array 204 through memory input/output circuitry 207 and...

37/3,K/17 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00317417 **Image available**
GRAPHICS CONTROLLER INTEGRATED CIRCUIT WITHOUT MEMORY INTERFACE
CIRCUIT INTEGRE POUR REGISSEURS GRAPHIQUES SANS INTERFACE MEMOIRE
Patent Applicant/Assignee:
  NEOMAGIC CORPORATION,
Inventor(s):
  PUAR Deepraj S,
  RANGANATHAN Ravi,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9535572 A1 19951228
  Application: WO 95US7196 19950605 (PCT/WO US9507196)
  Priority Application: US 94262412 19940620
Designated States: JP AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 7749

Main International Patent Class: **G11C-013/00**
Fulltext Availability:
  Detailed Description

Detailed Description
... 12 for manipulating video data, and a CPU interface 13, display interface 14 and video **memory** interface 15, The graphics **controller integrated circuit** 10 receives **video** image data from a CPU (central processing unit) through the CPU interface 13, and after processing the data, stores

that information through the **video** memory interface 15 in a separate **video** memory 11, also called the **video frame buffer**, The graphics controller 10 also makes sure that the image data is regularly retrieved from the **video** memory (through the interface 15) and fed to a display unit through the display interface...

...which satisfies the refresh requirements of the display, In some more advanced graphics controller systems, **video** image data may also be received from other sources, such as a device with a PCMCIA (Personal Computer **Memory** Card International Association) connector, The **video memory** interface 15 of the graphics **controller integrated circuit** 10 has ports dedicated to interface with the **video memory** 11, The number of ports required for this interface 15 is the sum of the address, data and control signals required to.access the **video** memory 11. The memory 11 has a size which is a function of the video...

?

```
File   2:INSPEC 1969-2004/Mar W3
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Mar W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Mar W3
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Mar W3
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Mar W4
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Mar W2
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File 144:Pascal 1973-2004/Mar W3
         (c) 2004 INIST/CNRS
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Apr
         (c) 2004 American Mathematical Society
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2004/Mar 30
         (c) 2004 ProQuest Info&Learning
File 248:PIRA 1975-2004/Mar W2
         (c) 2004 Pira International

Set     Items   Description
S1       4779   AU=(LAZAR P? OR YEO C? OR SELINGER D? OR KIM P? OR PINKHAM
             R? OR LAZAR, P? OR YEO, C? OR SELINGER, D? OR KIM, P? OR PINK-
             HAM, R?)
S2       1873   FRAME(3N)BUFFER?
S3         36   SENSE()AMPS
S4          0   S1 AND (S2 OR S3)
S5          0   S1 AND FRAME? AND BUFFER?
S6         11   S3 AND PY=1997:2004
S7         25   S3 NOT S6
S8         18   RD S7 (unique items)
```

8/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5173169 INSPEC Abstract Number: B9603-1265D-021, C9603-5320G-020
Title: An experimental 295 MHz CMOS 4K*256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**
Author(s): Kushiyama, N.; Tan, C.; Clark, R.; Lin, J.; Perner, F.; Martin, L.; Leonard, M.; Coussens, G.; Cham, K.
Author Affiliation: Semicond. Device Eng. Lab., Toshiba Corp., Kanagawa, Japan
Journal: IEEE Journal of Solid-State Circuits vol.30, no.11 p. 1286-90
Publisher: IEEE,
Publication Date: Nov. 1995 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
SICI: 0018-9200(199511)30:11L.1286:EC4S;1-5
Material Identity Number: I022-96001
U.S. Copyright Clearance Center Code: 0018-9200/95/$04.00
Language: English
Subfile: B C
Copyright 1996, IEE

Title: An experimental 295 MHz CMOS 4K*256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**
...Identifiers: bidirectional read/write shared **sense amps** ;

8/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5131868 INSPEC Abstract Number: B9601-1265D-028, C9601-5320G-024
Title: A 295 MHz CMOS 1 M (*256) embedded SRAM using bi-directional read/write shared sense amps **and self-timed pulsed word-line drivers**
Author(s): Kushiyama, N.; Tan, C.; Clark, R.; Lin, J.; Pemer, F.; Martin, L.; Leonard, M.; Coussens, G.; Cham, K.; Chiu, K.
Author Affiliation: Semicond. Device Eng. Lab., Toshiba Corp., Kanagawa, Japan
Conference Title: 1995 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.95CH35753) p. 304-5, 385
Editor(s): Wuorinen, J.H.
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 440 pp.
ISBN: 0 7803 2495 1
U.S. Copyright Clearance Center Code: 0 7803 2495 1/95/$4.00
Conference Title: Proceedings ISSCC '95 - International Solid-State Circuits Conference
Conference Date: 15-17 Feb. 1995 Conference Location: San Francisco, CA, USA
Language: English
Subfile: B C
Copyright 1995, IEE

Title: A 295 MHz CMOS 1 M (*256) embedded SRAM using bi-directional read/write shared sense amps **and self-timed pulsed word-line drivers**
...Identifiers: bi-directional read/write shared **sense amps** ;

8/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

4741933 INSPEC Abstract Number: B9410-1265D-006, C9410-5320G-004
Title: Large-signal 2T, 1C DRAM cell: signal and layout analysis
Author(s): Henkels, W.H.; Hwang, W.
Author Affiliation: T.J. Watson Res. Centre, IBM Res. Div., Yorktown Heights, NY, USA
Journal: IEEE Journal of Solid-State Circuits vol.29, no.7 p.829-32
Publication Date: July 1994 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
U.S. Copyright Clearance Center Code: 0018-9200/94/$04.00
Language: English
Subfile: B C

...Abstract: implementation employing a buried strap is proposed. Maximization of array density requires multiplexing bitlines to **sense amps** .

8/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02899998 INSPEC Abstract Number: B87037277, C87033726
Title: 1 Mbit CMOS EPROM: HN27C101 and HN27C301
Author(s): Fukuda, M.; Uchibori, K.; Meguro, S.
Author Affiliation: Musashi Works, Hitachi Ltd., Japan
Journal: Hitachi Review vol.35, no.5 p.263-6
Publication Date: Oct. 1986 Country of Publication: Japan
CODEN: HITAAQ ISSN: 0018-277X
Language: English
Subfile: B C

...Abstract: programming circuit are employed. These enable 4 bytes to be programmed at a time. The **sense amps** are improved in order to facilitate the detection of the small threshold voltage shift in...

8/3,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01848237 INSPEC Abstract Number: B82024519, C82018415
Title: A 30 ns 16K*1 fully static RAM
Author(s): Kang, S.D.; Allan, J.D.; Ashmore, B.; Herndon, T.H.; Wolpert, S.; Bruncke, W.C.
Author Affiliation: General Electric Co., Syracuse, NY, USA
Journal: IEEE Journal of Solid-State Circuits vol.SC-16, no.5 p. 444-8
Publication Date: Oct. 1981 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Subfile: B C

...Abstract: improve overall access times. One of the other major speed improvements came from utilizing column **sense amps** . The use of the column sense amp improves the overall speed by more than 20...
...Identifiers: column **sense amps**

8/3,K/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

01026288 INSPEC Abstract Number: B77009518, C77008899
Title: Radiation effects on commercial 4-kilobit NMOS memories
Author(s): Myers, D.K.
Author Affiliation: Fairchild Camera & Instrument Corp. Res. & Dev. Lab., Palo Alto, CA, USA
Journal: IEEE Transactions on Nuclear Science vol.ns-23, no.6 p. 1732-7
Publication Date: Dec. 1976 Country of Publication: USA
CODEN: IETNAE ISSN: 0018-9499
Conference Title: IEEE Annual Conference on Nuclear and Space Radiation Effects
Conference Sponsor: IEEE; Univ. Calif
Conference Date: 27-30 July 1976 Conference Location: San Diego, CA, USA
Language: English
Subfile: B C

...Abstract: by 3500 rads (Si). The entire circuit is dynamic including the peripheral circuitry with the **sense amps** detecting 200 millivolt signals. In the tested population, most failed for V/sub GT/ shifts...

8/3,K/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04331055 E.I. No: EIP96013007939
Title: Experimental 295 MHz CMOS 4K multiplied by 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**
Author: Kushiyama, Natsuki; Tan, Charles; Clark, Richard; Lin, Jane; Perner, Fred; Martin, Lisa; Leonard, Mark; Coussens, Gene; Cham, Kit
Corporate Source: Toshiba Corp, Kanagawa, Jpn
Source: IEEE Journal of Solid-State Circuits v 30 n 11 Nov 1995. p 1286-1290
Publication Year: 1995
CODEN: IJSCBC ISSN: 0018-9200
Language: English

Title: Experimental 295 MHz CMOS 4K multiplied by 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**

8/3,K/8 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04313566 E.I. No: EIP95122958419
Title: 286mm2 256Mb DRAM with X32 both-ends DQ**
Author: Watanabe, Y.; Wong, H.; Kirihata, T.; Kato, D.; DeBrosse, J.; Hara, T.; Yoshida, M.; Mukai, H.; Quader, K.; Nagai, T.; Poechmueller, P.; Pfefferl, K.; Wordeman, M.; Fujii, S.
Corporate Source: Toshiba, IBM, NY, USA

Conference Title: Proceedings of the 1995 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn   Conference Date: 19950608-19950610
E.I. Conference No.: 44078
Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers 1995. IEEE, Piscataway, NJ, USA,95CH35780. p 105-106
Publication Year: 1995
CODEN: 85PXA5
Language: English

Identifiers: Chip architecture; Hierarchical data line scheme; Boundary **sense amps** ; Peripheral circuits; Read-write data lines

8/3,K/9   (Item 3 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

04205698   E.I. No: EIP95072770194
Title: 295 MHz CMOS 1 M (x256) embedded SRAM using bi-directional read/write shared sense amps **and self-timed pulsed word-line drivers**
Author: Kushiyama, Natsuki; Tan, Charles; Clark, Richard; Lin, Jane; Perner, Fred; Martin, Lisa; Leonard, Mark; Coussens, Gene; Cham, Kit; Chiu, Kuang
Corporate Source: Hewlett-Packard Co, Palo Alto, CA, USA
Conference Title: Proceedings of the 1995 IEEE International Solid-State Circuits Conference
Conference Location: San Francisco, CA, USA Conference Date: 19950215-19950217
E.I. Conference No.: 43253
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference v 38 Febr 1995. IEEE, Piscataway, NJ, USA,95CH35753. 3p
Publication Year: 1995
CODEN: DTPCDE   ISSN: 0193-6530
Language: English

Title: 295 MHz CMOS 1 M (x256) embedded SRAM using bi-directional read/write shared sense amps **and self-timed pulsed word-line drivers**

8/3,K/10   (Item 4 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)

01233940   E.I. Monthly No: EIM8208-027448
Title: STATIC RAMs.
Author: Kang, S. Daniel; Allan, James D.; Ashmore, Buster; Herndon, Troy; Wolpert, Seth; Bruncke, William C.; Thorpe, Tom; Spicer, Julie
Corporate Source: Tex Instrum Inc, Houston, USA
Conference Title: Digest of Technical Papers - 1981 IEEE International Solid-State Circuits Conference.
Conference Location: New York, NY, USA   Conference Date: 19810218
E.I. Conference No.: 00350
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference v 24 1981. Publ by Lewis Winner, Coral Gables, Fla, USA. Also Available from IEEE Serv Cent (Cat n 81CH1588-3), Piscataway, NJ, USA p 18-19, 255
Publication Year: 1981
CODEN: DTPCDE
Language: English

Identifiers: STATIC RAMS; NMOS 16K RAM; DOUBLE-LEVEL POLYSILICON

TECHNOLOGY; SHARED CONTACTS; NMOS TRANSISTORS; COLUMN **SENSE AMPS** ; OUTPUT **SENSE AMPS**

8/3,K/11 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01182141 E.I. Monthly No: EI8203019749 E.I. Yearly No: EI82025795
Title: 30 ns 16K X 1 FULLY STATIC RAM.
Author: Kang, S. Daniel; Allan, James D.; Ashmore, Buster; Herndon, Troy H.; Wolpert, Seth; Bruncke, William C.
Corporate Source: GE, Syracuse, NY, USA
Source: IEEE Journal of Solid-State Circuits v SC-16 n 5 Oct 1981 p 444-448
Publication Year: 1981
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH

...Abstract: improve overall access times. One of the other major speed improvements came from utilizing column **sense amps** , which improved the overall speed by more than 20 percent. A write cycle of 30...

8/3,K/12 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05059001 Genuine Article#: TM391 No. References: 2
Title: AN EXPERIMENTAL 295 MHZ CMOS 4KX256 SRAM USING BIDIRECTIONAL READ/WRITE SHARED SENSE AMPS **AND SELF-TIMED PULSED WORD-LINE DRIVERS**
Author(s): KUSHIYAMA N; TAN C; CLARK R; LIN J; PERNER F; MARTIN L; LEONARD M; COUSSENS G; CHAM K
Corporate Source: TOSHIBA CO LTD,SEMICOND DEVICE ENGN LAB/KANAGAWA//JAPAN/; HEWLETT PACKARD CORP,HEWLETT PACKARD LABS/PALO ALTO//CA/94304; HEWLETT PACKARD CORP,INK JET BUSINESS UNIT/CORVALLIS//OR/97331; HEWLETT PACKARD CORP,INTEGRATED CIRCUIT BUSINESS DIV/PALO ALTO//CA/94304
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1995, V30, N11 (NOV), P 1286-1290
ISSN: 0018-9200
Language: ENGLISH Document Type: ARTICLE (Abstract Available)

Title: AN EXPERIMENTAL 295 MHZ CMOS 4KX256 SRAM USING BIDIRECTIONAL READ/WRITE SHARED SENSE AMPS **AND SELF-TIMED PULSED WORD-LINE DRIVERS**

8/3,K/13 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

00743461 Genuine Article#: ET301 No. References: 6
Title: ION MICROBEAM PROBING OF SENSE AMPLIFIERS TO ANALYZE SINGLE EVENT UPSETS IN A CMOS DRAM
Author(s): GEPPERT LM; BAPST U; HEIDEL DF; JENKINS KA
Corporate Source: IBM CORP,THOMAS J WATSON RES CTR,IBM RES DIV/YORKTOWN HTS//NY/10598
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1991, V30, N2, P132-134
Language: ENGLISH Document Type: NOTE (Abstract Available)

...Abstract: sense amplifiers dominate the SEU rate. This domination is due to the presence in the **sense amps** of n-channel devices which can collect charge from the entire ion track. In contrast...

8/3,K/14 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02340107 JICST ACCESSION NUMBER: 95A0545643 FILE SEGMENT: JICST-E
A 295MHz 4K word*256 bit SRAM using 0.3V swing I/Os.
KUSHIYAMA NATSUKI (1); TAN C (2)
(1) Toshiba Handotaidebaisukaiken; (2) Hewlett-Packard ULSI Lab., CA
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.71(ICD95 23-30), PAGE.55-61, FIG.12, TBL.1, REF.2
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

...ABSTRACT: in a 0.35.MU.m CMOS 4 metal layers process technology. Read/write shared **sense amps** which act as **sense amps** , write circuits, and data input level shifters to implement 256 pairs of I/Os. And...

8/3,K/15 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00968536 E96021246212
An experimental 295 MHz CMOS 4K x 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**
(Ein experimentelles 4K x 256 SRAM fuer 295 MHz in CMOS-Technik, das bidirektionale gemeinsame Schreib-/Lese-Verstaerker und gepulste Wortleitungs-Treiber nutzt)
Kushiyama, N; Tan, C; Clark, R; Lin, J; Perner, F; Martin, L; Leonard, M; Coussens, G; Cham, K
Toshiba Kanagawa, J; Hewlett-Packard, Palo Alto, USA; Hewlett-Packard, Corvalis, USA
IEEE Journal of Solid-State Circuits, v30, n11, pp1286-1290, 1995
Document type: journal article Language: English
Record type: Abstract
ISSN: 0018-9200

An experimental 295 MHz CMOS 4K x 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed word-line drivers**

8/3,K/16 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1390939 H.W. WILSON RECORD NUMBER: BAST96002551
An experimental 295 MHz CMOS 4K X 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed world-line drivers**

Kushiyama, Natsuki; Tan, Charles; Clark, Richard
IEEE Journal of Solid-State Circuits v. 30 (Nov. '95) p. 1286-90
DOCUMENT TYPE: Feature Article ISSN: 0018-9200

An experimental 295 MHz CMOS 4K X 256 SRAM using bidirectional read/write shared sense amps **and self-timed pulsed world-line drivers**

8/3,K/17 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

09625076 PASCAL No.: 91-0422182
Ion microbeam probing of sense amplifiers to analyze single event upsetsin a CMOS DRAM
GEPPERT L M; BAPST U; HEIDEL D F; JENKINS K A
IBM, Thomas J. Watson res. cent., res. div., YorktownHeights NY 10598, USA
Journal: IEEE journal of solid-state circuits, 1991, 26 (2) 132-134
Language: English

... sense amplifiers dominate the SEU rate. This domination is due to the presence in the **sense amps** of n-channel devices which can collect charge from the entire ion track. In contrast...

8/3,K/18 (Item 1 from file: 583)
DIALOG(R)File 583:Gale Group Globalbase(TM)

05380314
Intel sets data for fpga line
UK - INTEL TO LAUNCH FPGA LINE IN 1993
Electronics Times (ECT) 8 October 1992 p1

...10 ns pin-to-pin delays. The device consumes around 1.5 mA/MHz, and **sense amps** are kept running with a 5 mA minimum.
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